

CompactPCI®

# ICP-CM

Intel® Celeron® M Low  
Power CPU Boards



**GigaSTAR®**  
**PanelLink®**  
DIGITAL



## USER'S MANUAL

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MAN-ICP-CM

**inova®**  
Computers

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# Preface

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## Unpacking and Special Handling Instructions

This product has been designed for a long and fault-free life; nonetheless, its life expectancy can be severely reduced by improper treatment during unpacking and installation.

Observe standard antistatic precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces as these can cause short circuits, damage the batteries or disrupt the conductive tracks on the board.

Do not exceed the specified operational temperature ranges of the board version ordered. If batteries are present, their temperature restrictions must be taken into account.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, re-pack it as it was originally packed.

Before returning this product for repair, please ask for an RMA (Returned Material Authorization) number by submitting an email and supply the following information:

- Company name, contact person, shipping address and invoice address
- Product name and serial number
- Failure or fault description
- Clearly write the RMA number on the outside of the transportation carton.



## Revision History

Revision History			
Manual	MAN-ICP-CM		
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Issue	Brief Description of Changes	Author	Date of Issue
PD00941013.001	Preliminary, First Release; All pages revised	AB	26/07/2004

## Three Year Limited Warranty

**Inova Computers** ('**Inova**') grant the original purchaser of Inova products the following hardware warranty. No other warranties that may be granted or implied by anyone on behalf of **Inova** are valid unless the consumer has the expressed written consent of **Inova**.

**Inova** warrants their own products (excluding software) to be free from defects in workmanship and materials for a period of 36 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other consumers or long term storage of the product.

This warranty does not cover products which have been modified, altered, or repaired by any other party than **Inova** or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, misuse, incorrect handling, servicing or maintenance; or has been damaged as a result of excessive current/voltage or temperature; or has had its serial number(s), any other markings, or parts thereof altered, defaced, or removed will also be excluded from this warranty.

A customer who has not excluded his eligibility for this warranty may, in the event of any claim, return the product at the earliest possible convenience, together with a copy of the original proof of purchase, a full description of the application it is used on, and a description of the defect; to the original place of purchase.

Pack the product in such a way as to ensure safe transportation (we recommend the original packing materials), whereby **Inova** undertakes to repair or replace any part, assembly or sub-assembly at our discretion; or, to refund the original cost of purchase, if appropriate.

In the event of repair, refund, or replacement of any part, the ownership of the removed or replaced parts reverts to **Inova**, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" returned from **Inova** with the repaired or replaced item.

Other than the repair, replacement, or refund specified above, **Inova** will not accept any liability for any further claims which result directly or indirectly from any warranty claim. We specifically exclude any claim for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time. The extent of **Inova's** liability to the customer shall not be greater than the original purchase price of the item for which any claim exists.

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# Product Overview

1

## Overview Contents

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## 1.0 ICP-CM CPU

**1**

Cutting edge technology makes the Inova Socket mPGA479M, Celeron® M single-board computer the ideal controller for a wide range of embedded (low power) industrial automation, military, medical, aerospace, imaging, telecommunications, process control and embedded/OEM applications. Without altering the design, Master or Slave ICP-CM CPUs can be operated in an industrial environment through their ability to detect automatically the backplane system controller or peripheral slot. In addition, the ICP-CM family can communicate at very high speed with up to 255 x 7 cascaded peripherals like graphics, industrial I/O or fast data acquisition modules on inter-linked passive backplanes.

The powerhouse in any application, Inova's Socket mPGA479M based high-performance 3U CompactPCI CPU is packed with a feature set unrivalled in industry on such a small scale. Configured with up to 1GByte onboard 266MHz DDR SDRAM, the ICP-CM is the ideal choice for low-power, high performance computing tasks. In addition, enriched performance scalability is assured through the latest Intel® Celeron® M processors and board feature set. Conforming to the latest PICMG CompactPCI specification the ICP-CM has a colourful feature set that includes rear I/O options, choice of graphic components and flexible mass-storage expansion options.

Being of a true universal design, both 5.0 and 3.3V I/O signalling voltages are possible without board modification. The auto-detect mechanism in the PCI/PCI bridge permits the same CPU to operate as a system Master controller or reside in a peripheral slot. A Slave CM CPU is thus able to communicate with the host controller through the bridge via the CompactPCI backplane (for high-speed DMA for example) or front-panel TCP/IP.

The standard Inova ICP-CM configuration is ready to run - straight from the box. Utilizing the low-power consumption and the high-performance of the Celeron processor enables truly embedded, ruggedized industrial applications to be engineered utilizing the latest software available today. 512kByte of L2 cache backed by up to a 1GByte bank of soldered double-data rate (DDR) SDRAM clocked at 266MHz ensures an efficient processor-level data throughput exceeding that of any comparable product.

For hard-core ruggedized applications, and thanks to the miniaturisation of silicon components, Inova's engineers have squeezed in a Compact FLASH socket suitable for use by all 3rd party Micro-Drive devices or solid-state FLASH that adhere to the interface standard.

Serviceability and user friendliness feature throughout the CPU design and is highlighted in the lack of on-board cabling - all interconnects are hard-wired. An optional dedicated hard disk carrier with integrated COM ports, twin USB 2.0 and PS-2 mouse and keyboard interfaces connects directly to the base CPU. Naturally, for space critical applications, these interfaces are available as rear I/O - effectively extending the standard 160mm card by a further 80mm! Notebook hard disks are selected for their high capacity, small footprint, rugged operating conditions and higher operational temperature characteristics.

## 1.01 Interfacing

To satisfy today's LAN-hungry industrial applications, Inova have implemented dual, independent 100BaseTx LAN Fast Ethernet interfaces as standard on the CPU's front-panel - or fed to a rear I/O transition module on the backplane. Connectivity is further enhanced through the integration of the latest USB 2.0 serial interfaces that permit a number of readily available peripherals such as mouse, keyboard, floppy drives and even CD-ROMs or printers to be utilized without compromising front panel width.

## 1.02 Peripherals

The ICP-CM supports standard PC peripherals – floppy disk, hard disk and CD ROM. Notebook style hard disks may be connected directly to the base-board (2-slot) and possess their own front-panel offering COM ports and combined PS-2 style connector for mouse and keyboard.

## 1.03 Software

The following operating systems are compatible with Inova's CM, 3U CompactPCI CPU:

- Linux
- Windows® 2000
- Windows® XP
- Windows® NT® & VenturCom RTX® (Real-Time Extension) - On request
- Windows® CE - On request
- Windows® 9x - On request
- Windriver VxWorks® - On request
- QNX® - On request
- Esmeralda Technology Jbed® (under development - On request)
- Solaris x86 - On request

All readily available application software designed for operation on the standard x86 architecture will execute without modification.

## 1.04 Graphics

Built in to the ICP-CM chipset is an analog VGA interface with BIOS configurable video RAM allocation extracted from the system memory.

Inova have also developed a number of ATI Radeon R7000-based dedicated AGP plug-in modules complete with video controller and RAM etc. for graphic intensive applications or to provide greater display flexibility.

Depending on the selected module, MPEG-2 decoding, sound functions, GigaST★R for distributed display communication, PanelLink or TFT flat-panel connectivity can be easily implemented.

## 1.1 Specifications

1

<b>Processor</b>	600MHz or 1.3GHz Socket mPGA479M mobile Intel Celeron M with 400MHz PSB, 512kByte L2 cache, passive or active cooling
<b>Memory</b>	Either 256MByte or 1GByte soldered 266MHz DDR SDRAM
<b>FLASH Socket</b>	For CompactFlash devices (Flash & MicroDrives) providing >4GByte mass-storage capacity
<b>Phoenix BIOS Ver. 4.x Rel. 6.0</b>	<ul style="list-style-type: none"> <li>▶ LAN Boot</li> <li>▶ ACPI 2.0</li> <li>▶ Multi Boot</li> <li>▶ USB Boot</li> <li>▶ Quick Boot</li> <li>▶ Quiet Boot</li> </ul>
<b>Battery</b>	Lithium cell for RTC (NV-RAM) with a lifetime > 10 years
<b>Host Bridge</b>	SiS651 North Bridge supporting <ul style="list-style-type: none"> <li>▶ 400/533MHz FSB to CPU</li> <li>▶ 333MHz, 64-bit DDR DRAM controller</li> <li>▶ VGA interface (2048 x 1536 pixels)</li> <li>▶ AGP 4x interface</li> <li>▶ Power management</li> </ul>
<b>South Bridge</b>	SiS962 <ul style="list-style-type: none"> <li>▶ PCI Bus 32-bit / 33MHz</li> <li>▶ Mouse &amp; keyboard controller</li> <li>▶ Fast Ethernet</li> <li>▶ USB 2.0</li> <li>▶ AC97 bus (sound)</li> <li>▶ LPC bus to Super I/O &amp; BIOS</li> <li>▶ IDE Controller (2 independent IDE channels - each supporting 2 devices)</li> <li>▶ Ultra DMA 133 support</li> <li>▶ Real-Time Clock</li> <li>▶ Watchdog - programmable up to 256 hours; issues SMI or Reset</li> <li>▶ Interrupt controller</li> <li>▶ Power Management Unit</li> </ul>
<b>Super I/O</b>	PC87393: <ul style="list-style-type: none"> <li>▶ Floppy Disk Controller, 1 Parallel Port (ECP, EPP), 2 serial COM Ports</li> <li>▶ Watchdog</li> </ul>
<b>Graphic Option</b>	Onboard video controller (chipset) with: <ul style="list-style-type: none"> <li>▶ BIOS selectable video RAM allocation</li> <li>▶ Support for MPEG-2 video playback</li> <li>▶ Support for VESA standard super high resolution graphics modes</li> <li>▶ Support for low-resolution modes (320x240, 512x384, 400x300)</li> <li>▶ Supports VESA Display Power Management Signalling</li> <li>▶ Supports Direct Draw Drivers</li> <li>▶ Supports single video windows with overlay function</li> </ul> or AGP 4x Piggyback (R7000) with: <ul style="list-style-type: none"> <li>▶ 32MByte RAM</li> <li>▶ 3D graphics, DVD &amp; MPEG-2 support</li> <li>▶ Multi-Display</li> <li>▶ PanelLink &amp; TFT support</li> <li>▶ GigaSTAR support</li> <li>▶ Sound support</li> <li>▶ Dual View support under Microsoft Windows 9x, Windows 2000 &amp; XP</li> <li>▶ CRT / TFT resolutions up to 2048x1536</li> </ul>

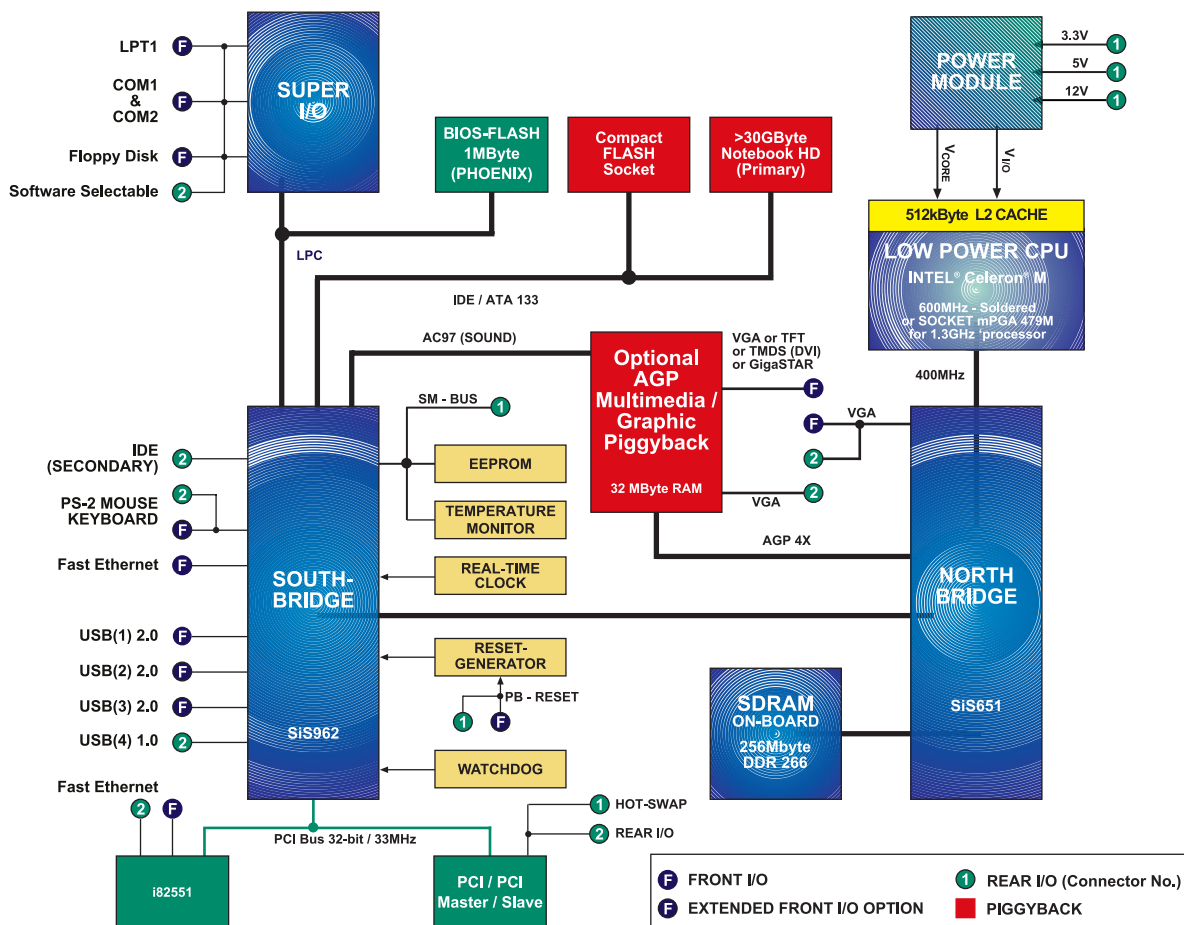
<b>Fast Ethernet</b>	Additional 82551 controller
<b>PCI/PCI</b>	Universal bridge (Master or Slave) <ul style="list-style-type: none"><li>▶ Serialized interrupts</li><li>▶ Universal (3.3/5.0V) V I/O support</li><li>▶ 32-bit and Rear I/O</li></ul>
<b>On-Board I/O</b>	<ul style="list-style-type: none"><li>▶ Dual 10/100 Mbit/s Fast Ethernet</li><li>▶ 1x front-panel 480Mbit/s, USB 2.0, (1x rear-panel 12Mbit/s, USB 1.1)</li><li>▶ VGA (chipset or AGP)</li></ul>
<b>Rear I/O</b>	Standard to all CPU variants is option 'D': <ul style="list-style-type: none"><li>▶ VGA (chipset or AGP if installed)</li><li>▶ Fast Ethernet ETH 1 (Intel 82551)</li><li>▶ USB 1.1</li><li>▶ PS-2 mouse &amp; keyboard</li><li>▶ 2<sup>nd</sup> IDE channel (Master &amp; Slave)</li><li>▶ Software configurable<ul style="list-style-type: none"><li>▶ LPT1 or</li><li>▶ COM1 &amp; COM2 or</li><li>▶ Floppy disk (A or B - BIOS selectable)</li></ul></li><li>▶ Reset &amp; Beeper</li></ul>
<b>Mass Storage</b>	1.44MByte 3.5" floppy drive and EIDE (standard 40-pin header - 80-strand ATA-5 compatible) supporting 2 pairs (Master/Slave) hard-disks or CD ROMs
<b>Front-Panels</b>	8HP front-panel with 2x USB 2.0, COM1, COM2, combined PS-2 mouse & keyboard; 12HP panel has LPT
<b>Connectors</b>	USB (USB), 2x RJ45 (Ethernet), 9/15-pin D-Sub (Graphic piggyback) or 15-pin high-density D-Sub (VGA)
<b>CompactPCI</b>	<ul style="list-style-type: none"><li>▶ Universal (transparent/non-transparent) PCI/PCI bridge for Master/Slave operation</li><li>▶ PICMG 2.0 R3.0, 32/64-bit, 33MHz system slot interface with 7 Master (DMA) support.</li><li>▶ Full Hot-Swap according to PICMG2.1 R2.0</li></ul>
<b>Mechanics</b>	3U (100 x 160mm) x 21/42mm (4TE/8TE)
<b>Power Cons.</b>	Typ. 15W
<b>Software Support</b>	Windows®XP, Windows®2000, Windows®NT, Windows®9x, Linux, VxWorks®, QNX®, OS9
<b>Mass</b>	220g (4TE)
<b>MTBF</b>	>220,000 hours @ 20°C
<b>Oper. Temp.</b>	0°C to +65°C (Std.) -40°C to +85°C (Opt.) Passive cooling requires - refer to Table 1.51 for details
<b>Storage Temp.</b>	-40°C to +85°C
<b>Humidity</b>	5% to 95% (non-condensing)
<b>Warranty</b>	Three-year limited warranty
<b>Conformance</b>	PICMG 2.0 R3.0; CE

\*Notes: CPUs fitted with HD, FD or CD-ROM etc. have a max. operational temp. of 50°C.  
Rear I/O D necessitates backplanes being PICMG 2.0 Rev. 3.0 compatible



## 1.2 Functional Overview

Figure 1.20 ICP-CM Interfacing

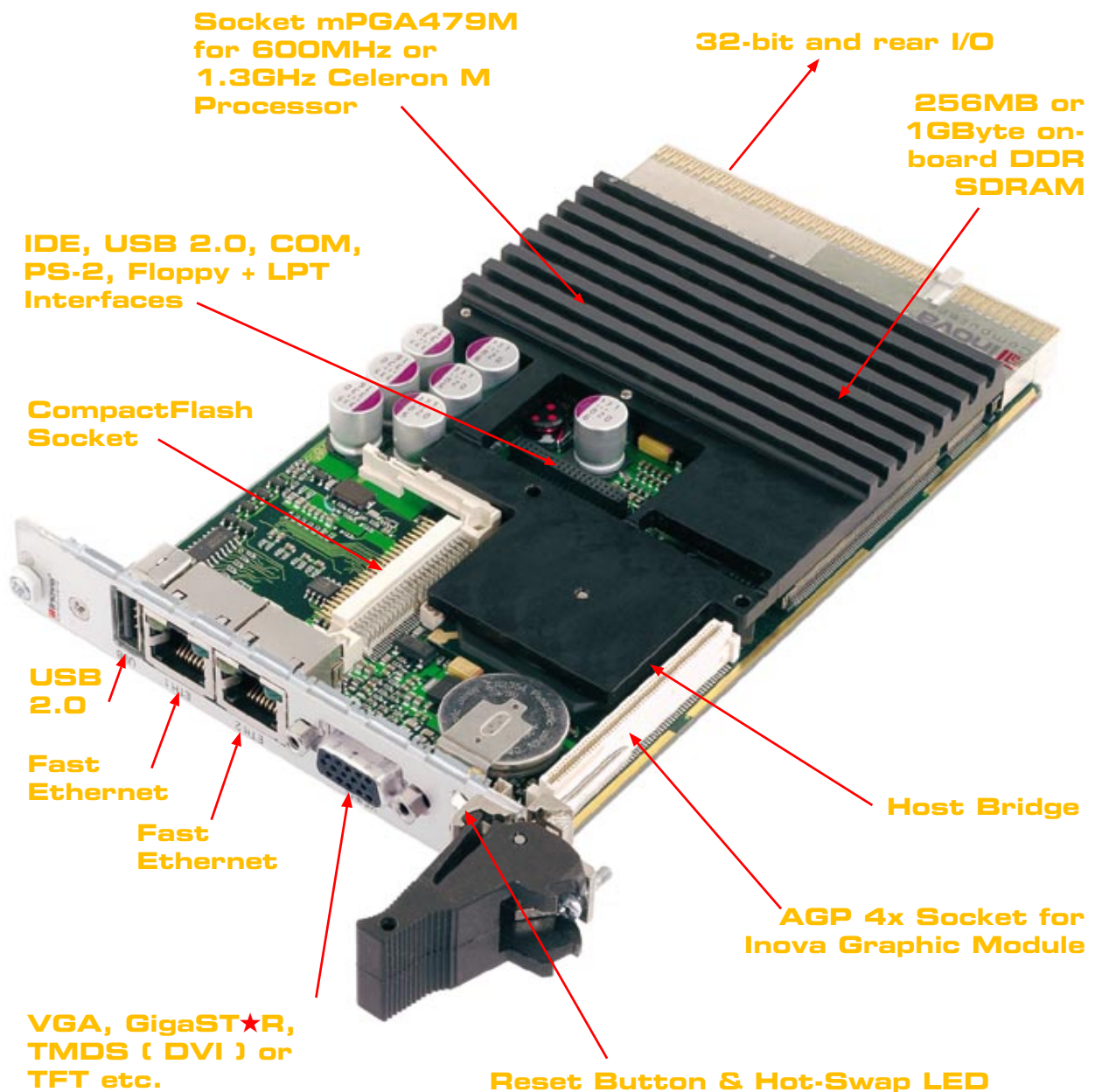


Inova's CPUs have been prepared for rear I/O operation. Currently RIO-D is supported with VGA, single-channel Fast Ethernet, second EIDE channel, USB 1.1, mouse, keyboard, reset and loud-speaker (beeper) and a software selectable choice between LPT1, COM1 & COM2 or floppy drive.

Other rear I/O options may also be available (including customer specific) but are not referred to in this user's handbook. For OEM quantities and compatibility with existing 2.11 backplanes etc. RIO-C1 could be considered - this is identical to rear I/O (D) except that the VGA, COM and PS-2 mouse options are not available. In order to take full advantage of the rear I/O features, the CompactPCI backplane needs to support them. Inova provides two standard versions; the first has the rear rP2 connector on the Master CPU slot only while the other has all slots fitted with rP2 connectors.

Be aware that boards using the PXI bus will experience signal conflict if used with any (includes non Inova boards) CPU offering rear I/O - Therefore, in such cases always select a CPU board configuration without rear I/O. Also, for compatibility with older backplane revisions (2.11), rear I/O (C) should be selected if indeed rear I/O is required. CPUs configured with rear I/O (D) will not work!

Figure 1.21 ICP-CM Board Overview



## **1.3 Software**

### **1.31 Windows XP (Professional / Embedded)**

Windows XP (Professional / Embedded) contains many new technologies and features designed for businesses of all sizes and for users who demand the most from their computers. It integrates the strengths of Windows 2000 (Professional), such as standards-based security, manageability and reliability, with Plug and Play convenience, simplified user interfacing, and innovative support services. This combination creates the best desktop operating system for businesses. Whether Windows XP (Professional) is installed on a single computer or deployed throughout a worldwide network, this new operating system increases computing power while lowering the cost of ownership for desktop computers.

### **1.32 Windows 2000 (Professional)**

Windows 2000 is highly reliable and available 32-bit OS which provides support for USB devices and permits connection of peripherals without the need to reboot the system. Unlike Windows NT 4.0, support is also provided for the IEEE1394a (FireWire) devices. Finally, secure, wireless communication between two Windows 2000-based computers is possible using the popular IrDA infrared protocol.

Removable storage devices such as DVD and Device Bay are supported as are new display devices such as Accelerated Graphics Port (AGP), multiple video cards and monitors, OpenGL 1.2, DirectX® 7.0 API, and Video Port Extensions. With Plug and Play, automatic installation of new hardware is possible with only minimal configuration. More than 12,000 devices support this functionality.

### **1.33 Linux**

Being a modern operating system, Linux executes a 32-bit architecture, uses pre-emptive multitasking, has protected memory, supports multiple users, and has rich support for networking, including TCP/IP. Linux was originally written for Intel's 386 architecture, but now runs on a wide variety of hardware platforms including the full x86 family of processors as well as Alpha, SPARC, and PowerPC.

Linux's architecture also creates a more reliable and inherently stable system through the use of protected memory and pre-emptive multitasking. Protected memory prevents an error in one application from bringing down the entire system, and genuine multitasking means that a bottleneck in one application does not hold up the entire system. Linux also maintains a very clean separation between user processes and kernel processes. While other server class operating systems use protected memory this feature is prone to failure if faulty applications are allowed to invade kernel space with their processes.

### **1.34 VentureCom**

Hard, real-time scalability and embedded operation extensions are required for Windows NT by HAL modification for deterministic interrupt handling at multiple priority levels. This approach achieves response times in the  $\mu$ s range and reduces hardware resource requirements while maintaining full compatibility with the enormous range of standard software and device drivers written for the Windows NT operating system.

## 1.35 Windows CE

Microsoft® Windows CE is an operating system designed for a wide variety of embedded systems and products, from hand-held PCs and consumer electronic devices to specialized industrial controllers and embedded communications devices. The Windows CE operating system has proved itself capable of handling the most demanding 32-bit embedded applications by bringing the full power of the Microsoft's 32-bit programming and operating systems technology to the embedded systems designer. Windows CE is actually a collection of operating system modules and components that can be selected and configured to meet the needs of a specific embedded application or product.

## 1.36 VxWorks

WindRiver's run-time system solution is a high-performance RTOS with a scalable microkernel and sophisticated networking facilities - like TCP/IP networking across various media.

The open architecture provides efficient support of PC-based architectures. Flexible, intertask communication,  $\mu$ s interrupt handling, POSIX 1003.1b real-time extensions, fast and flexible I/O system etc. are some of the many key features.

## 1.37 OS-9 x86

Microware's real-time operating system has a track record that has been proved in the industrial/embedded market and has continued to provide reliable intelligence to sophisticated applications. OS-9 x86's flexibility, modularity and reliability in conjunction with a rich driver structure allow its use in I/O intensive applications.

## 1.38 QNX

This solution ports the Win32 API to a QNX kernel. The Win32 API aims to define a standard for developing open systems applications that are optimized to run on 'Wintel' platforms. This operating system evolves around a small microkernel RTOS that produces a protected-mode, POSIX-certified API. Being fully modular and scalable, this technology creates the smallest footprint that is beneficial to high-end server applications.

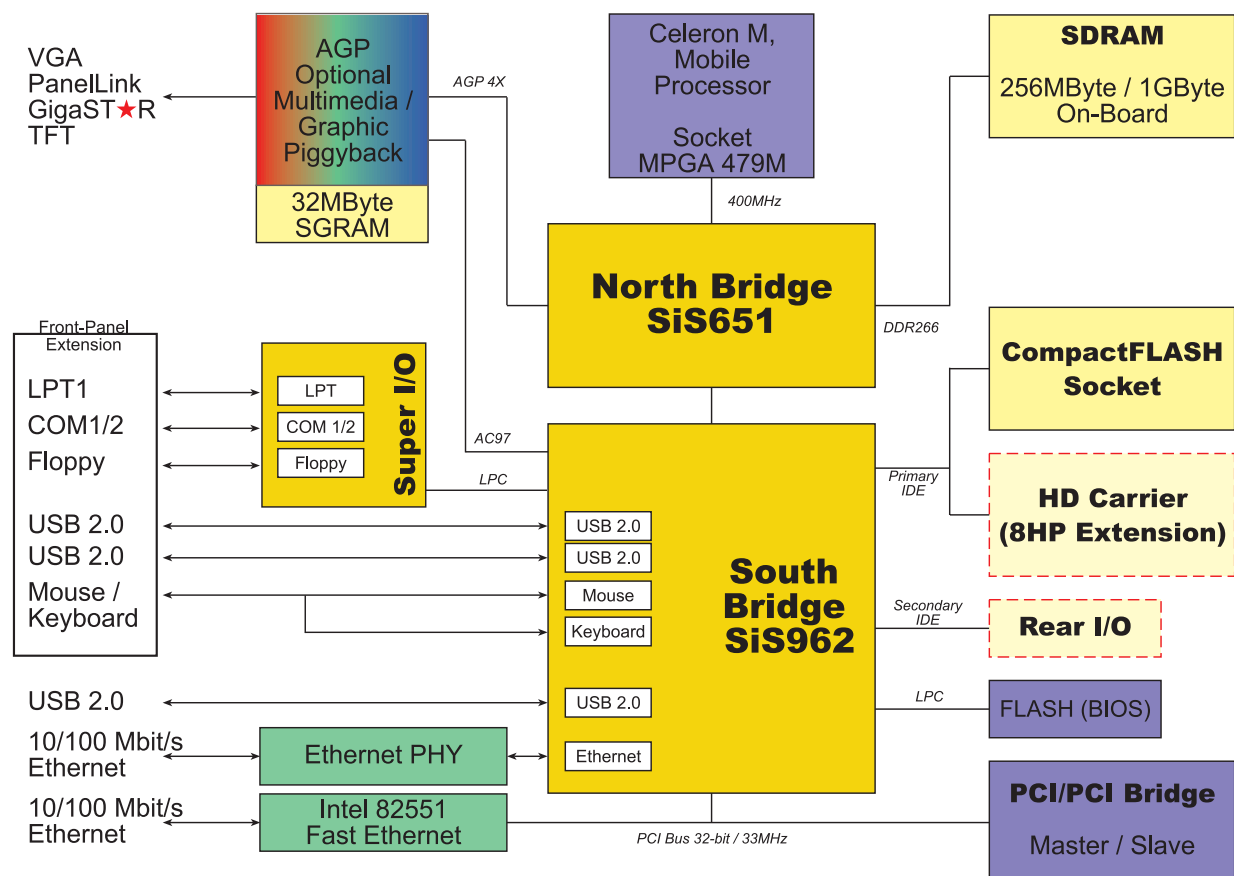
## 1.39 Jbed

Esmertec's Jbed is a new generation of real-time operating system. Java-based innovation provides unprecedented safety and ease of use without compromising resource efficiency (native processor speed) or hard real-time performance. In addition, advanced features are implemented such as modularity, hot updates, deadline-driven scheduling admission testing as well as a fast and productive cross-development.

## 1.4 Hardware

### 1.41 Block Diagram

Figure 1.41 Block Diagram



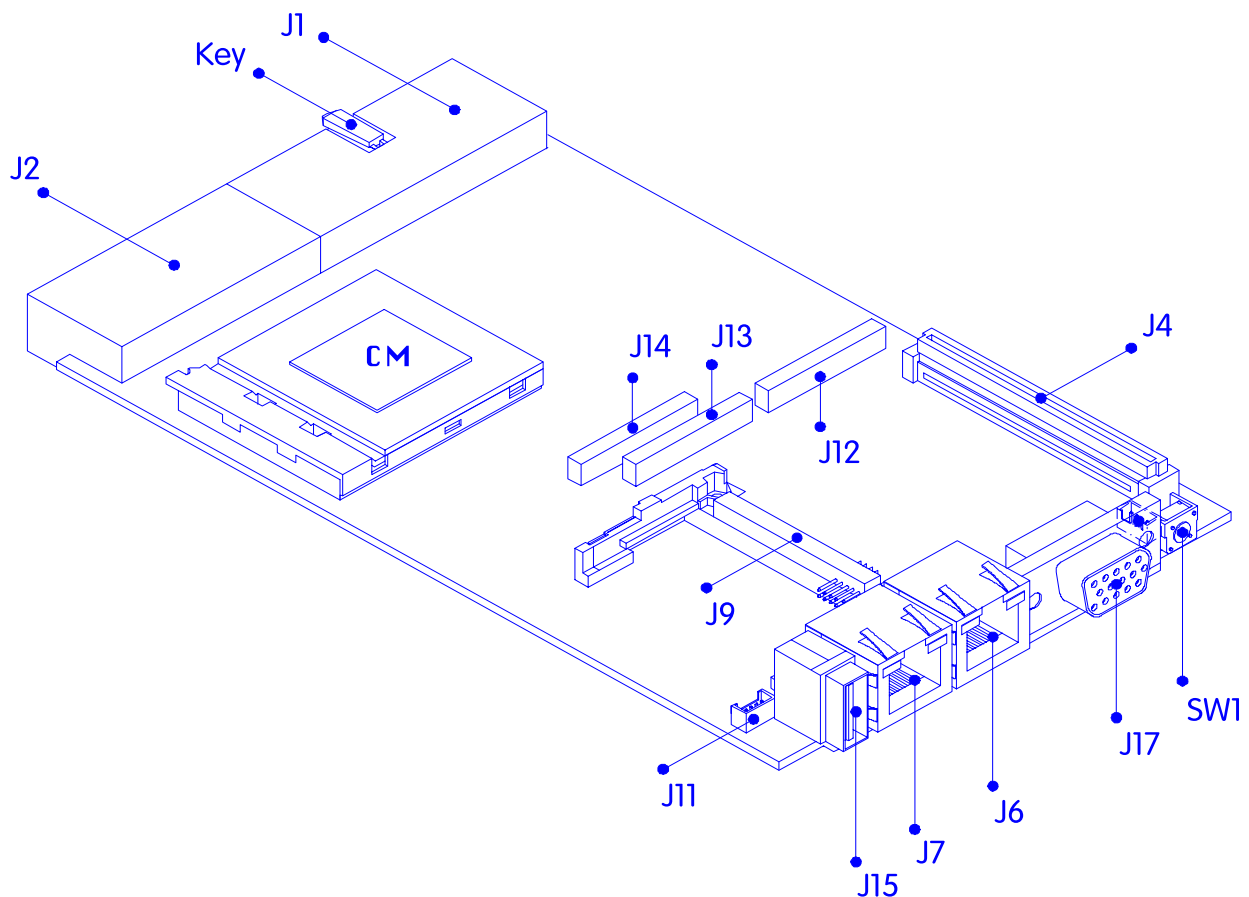
This block diagram is applicable to all Inova's CM-based CPUs. Components and/or functionality may change without notice.

#### Note

32-bit with or without Rear I/O (RIO) configurations are possible. User's of NI peripheral cards should check to see whether signal conflict is possible with the RIO option selected. If in doubt, select the CPU version without RIO. The universal PCI/PCI bridge allows the CPU to exist as a Master or Slave. Recognition is automatic depending on the CPU's physical position within a CompactPCI system.

## 1.42 Connector Location

Figure 1.42 Connector Locations



## 1.43 Connector Description

Table 1.43 Connector Description

Connector	Description
J1, J2	CompactPCI Interface Connector
J4	AGP 4x for Optional Inova Graphic Piggyback
J6	10BaseT/100BaseTx Fast Ethernet Interface ETH2 - [SiS 900 - chipset]
J7	10BaseT/100BaseTx Fast Ethernet Interface ETH1 - [i82551]
J9	CompactFlash Socket (MicroDrive or Flash)

Table 1.43 Continued

Connector	Description
J11	Internal USB (1.1) interface for additional USB devices (USB 5)
J12, J13, J14	Hard Disk module, Mouse, Keyboard, COM, FD, USB 2.0 and LPT1 interfaces
J15	External USB 2.0 interface (USB 1)
J17	VGA interface (soldered D-Sub for onboard Chipset or from AGP piggyback)
SW1	Reset button switch

## 1.44 Front-Panel Features

Table 1.44 Front Panels

Interface	Description & Location
Ethernet	2x RJ45 connector common to all CPU front-panels
USB	USB (2.0) connector on all CPU front-panels (USB 1)
VGA	Space for 15-Pin high-density D-Sub connector on all CPU front-panels
Reset	Push-button reset on all CPU front-panels

### Extended Front Panel Options - 8HP & 12HP

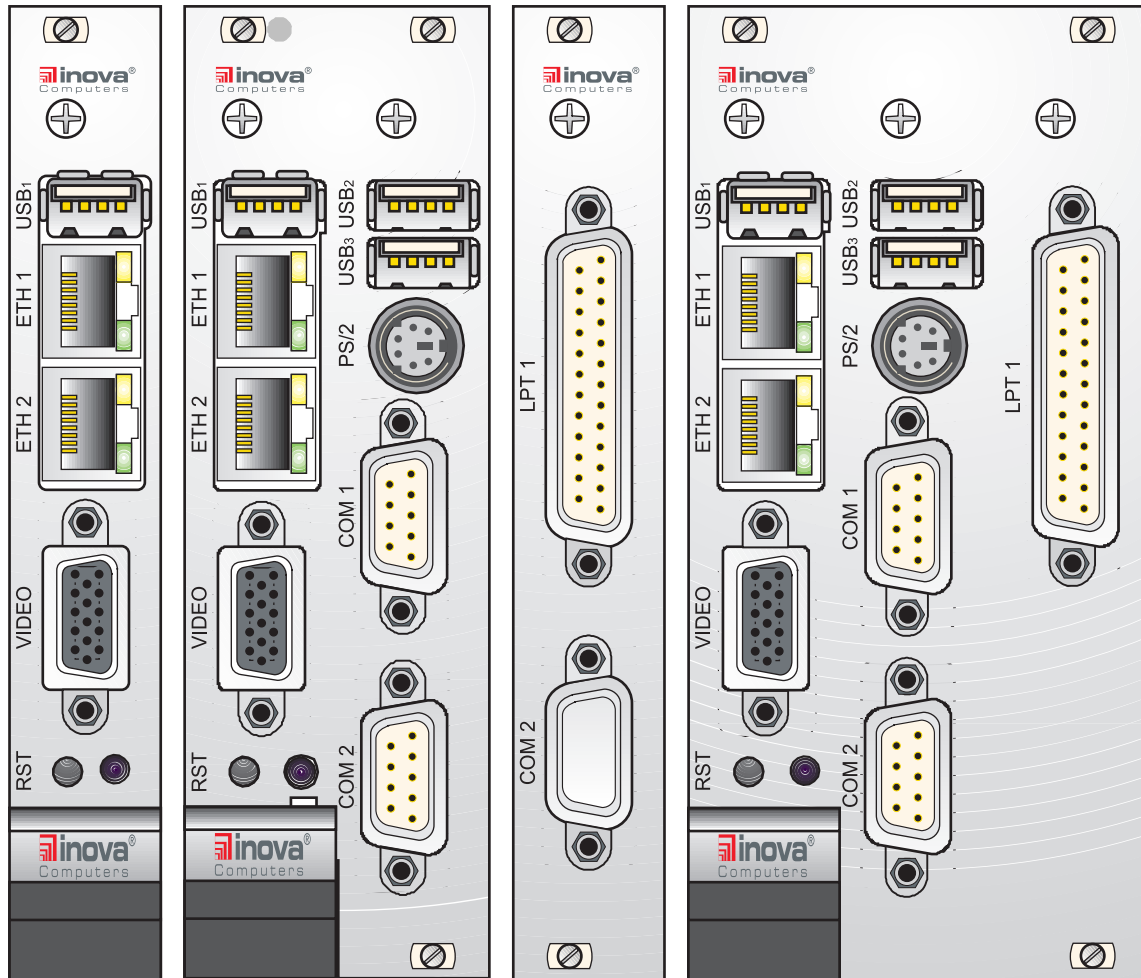
Mouse & Keyboard	Single PS-2 style connector
USB	Two USB 2.0 connectors (USB 2 & USB 3)
COM1 <sup>1)</sup>	9-Pin D-Sub
COM2 <sup>1)</sup>	9-Pin D-Sub
LPT1	25-Pin D-Sub integrated within the 12HP panel only
Floppy	Standard (notebook) header for slim-line floppy interface

#### Note

<sup>1)</sup> The ICP-CM Hard Disk carrier - ICP-HD3 (Refer to Appendix A) has jumper selectable COM configurations - either RS232 or RS485



Figure 1.44 Front-Panel Options



The front-panels shown in Figure 1.44 show the tremendous flexibility built into Inova's CPU concept. From left, the standard CPU is 4TE with dual Fast Ethernet, USB (2.0) and VGA graphic connections. If, instead of VGA graphics, PanelLink or GigaST★R is required then an AGP piggy-back is installed on J4 for this purpose. TFT graphics are realised in a similar way except the front-panel will be cut away (to the right of the VGA connector) to permit passage of the flat-band ribbon cables.

If the application requires a PS/2 mouse, PS/2 keyboard, floppy, COM or LPT ports or if the CPU is equipped with a hard disk, IDE FLASH or an adapter that accesses other devices attached to this primary IDE channel, then an 8TE front-panel is selected. Both COM ports (jumper selectable to be RS232 or RS485) are installed on Inova's ICP-HD-3 carrier board as are the interfaces for the LPT and slim-line FD.

The LPT interface is available on a dedicated panel shown to the right of Figure 1.44.



## 1.45 Interface Positions

Figure 1.45 Interfaces

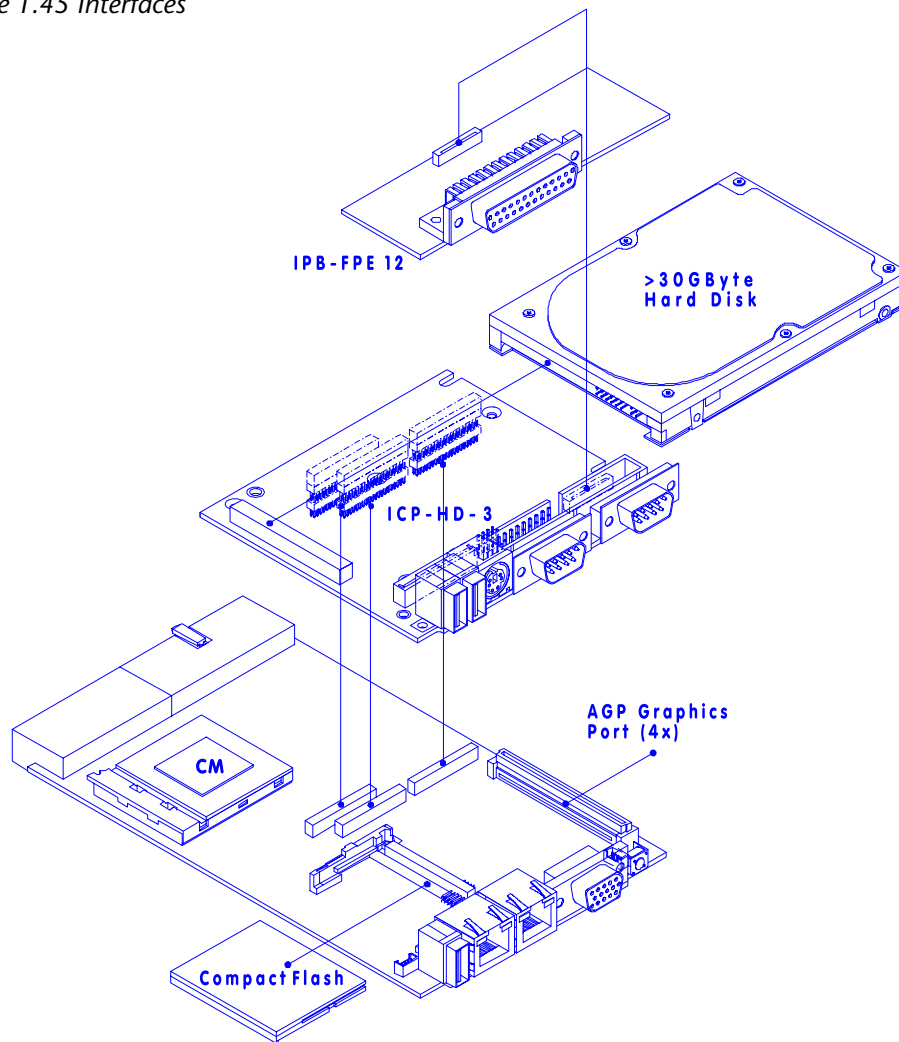


Figure 1.45 shows the typical positioning of the front panel extension modules for mouse, keyboard, COM1, COM2, and LPT interfaces.

### Note

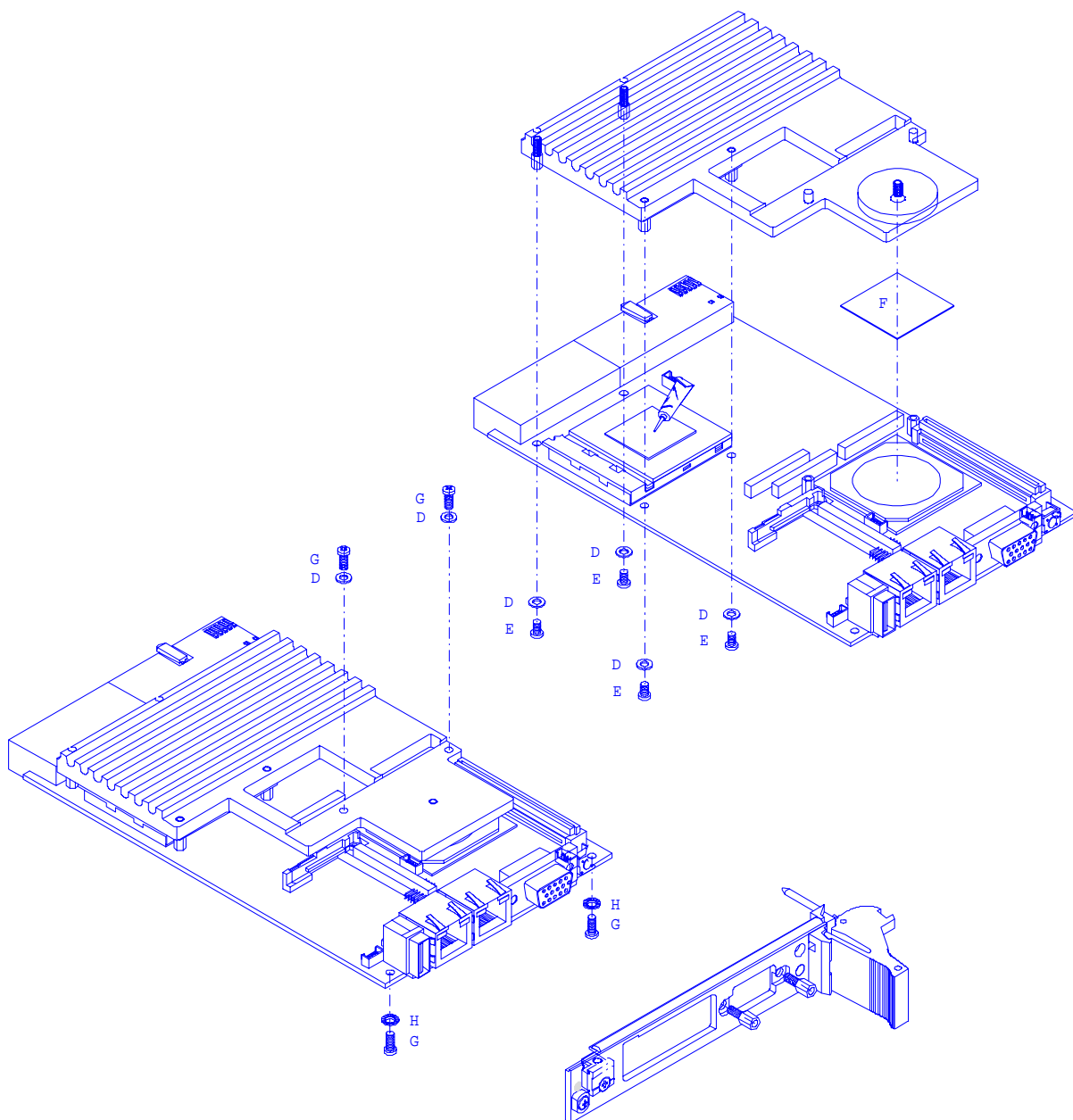
*A hard disk, if installed, will generally be fitted to the piggyback containing the combined PS-2 mouse / keyboard, USB2.0, COM1 and COM2 interfaces.*

## 1.46 Construction - 4HP Standard CPU

This standard CPU configuration comprises:-

- Passively cooled base with chipset VGA graphics, dual Fast Ethernet and single USB 2.0 interface for mouse, keyboard, FD, CD-ROM etc. The minimum airflow requirements must be compatible with the selected 'processor speed, CPU damage could result otherwise !

Figure 1.46 Construction of CPU with Heat-Sink Assembly

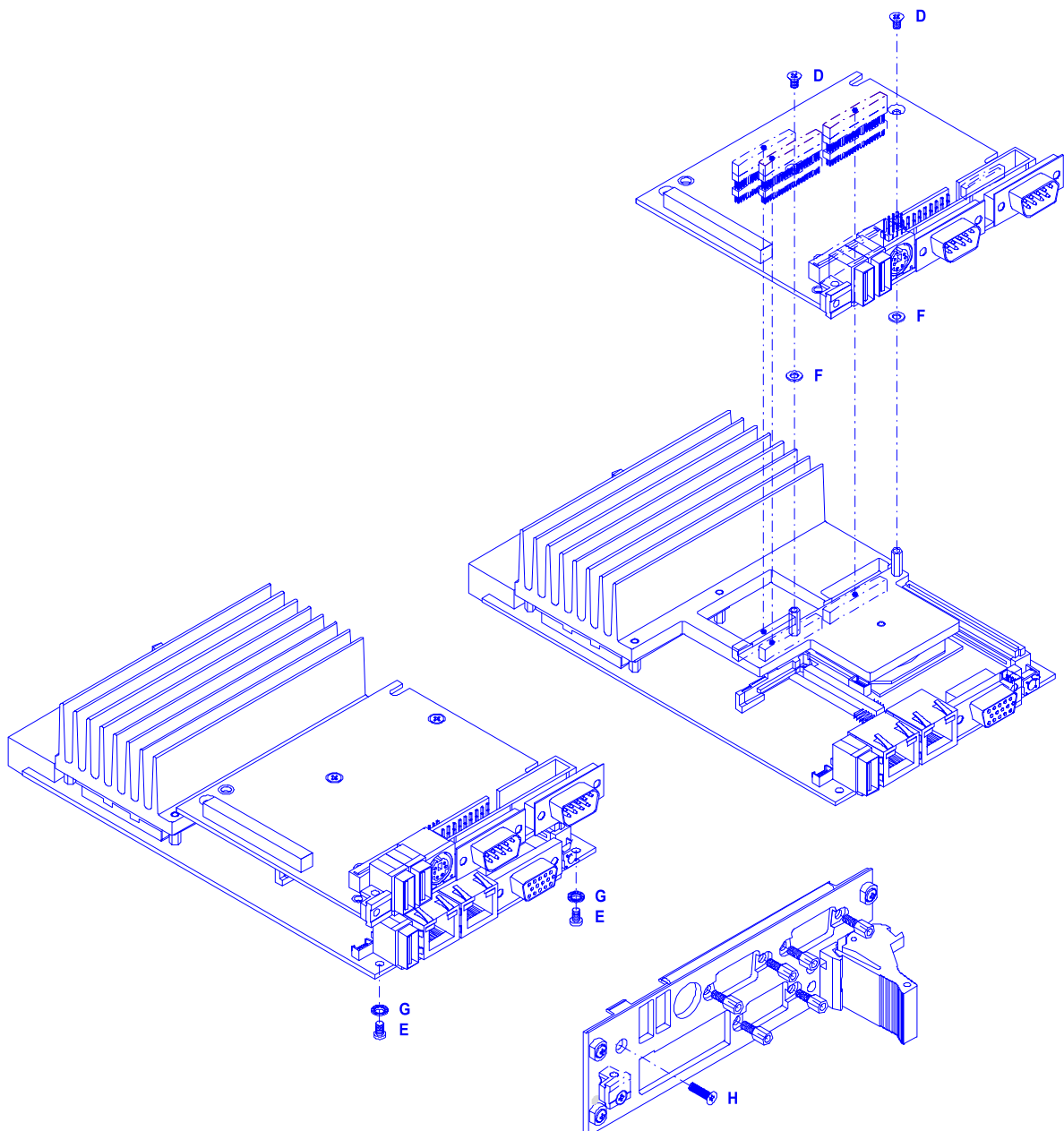


## 1.47 Construction - 8HP Standard CPU

This standard CPU configuration comprises:-

- Passively cooled base with chipset VGA graphics, dual Fast Ethernet, three USB 2.0 interfaces, combined PS-2 mouse / keyboard, COM1 and COM2 interfaces. Behind the extended front-panel is a platform for any IDE HD or Flash device with additional interfacing for FD and LPT - refer to Appendix A for further information. The minimum airflow requirements must be matched with the selected 'processor speed, CPU damage could result otherwise !

Figure 1.47 Construction of CPU with Heat-Sink Assembly

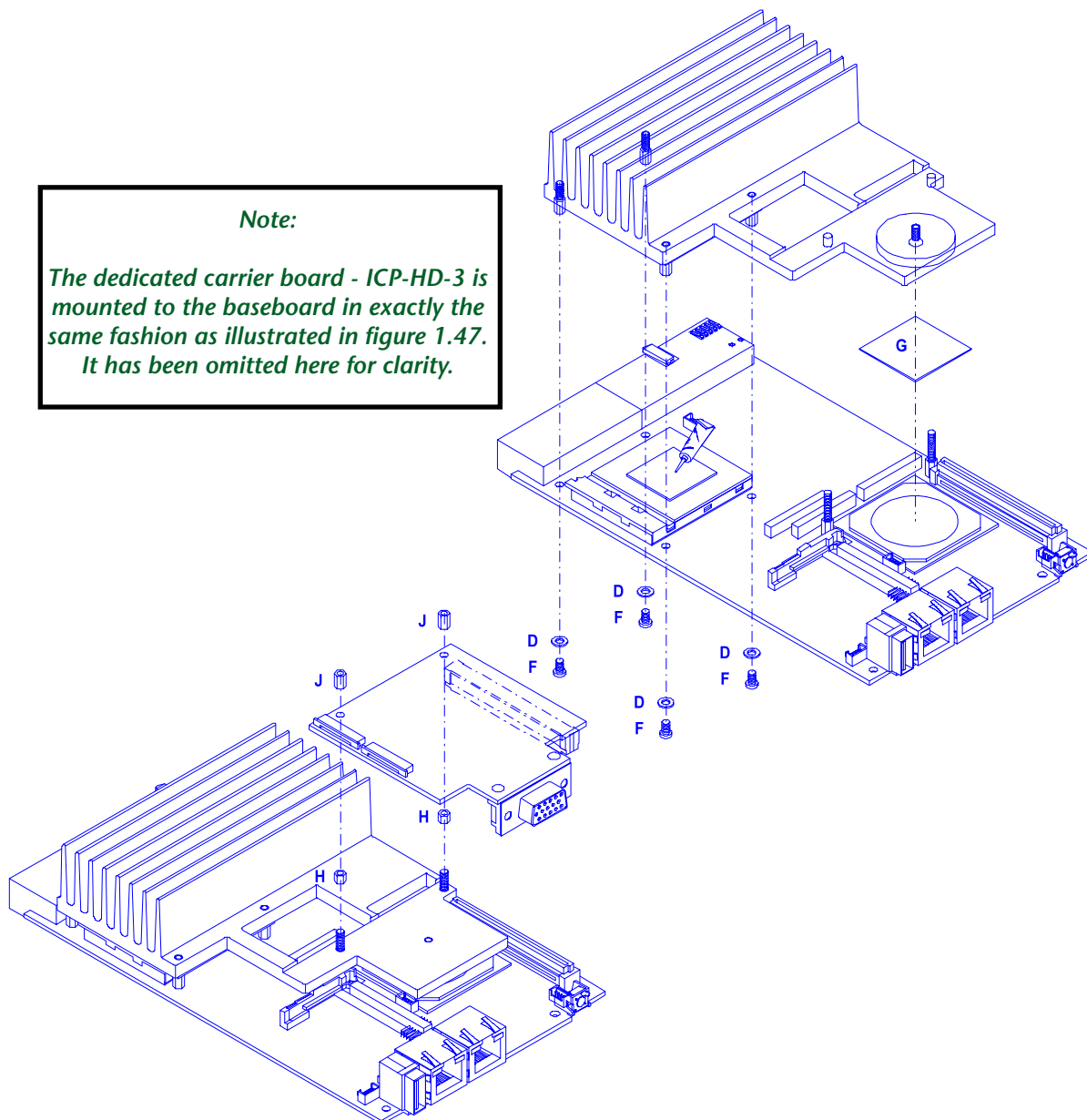


## 1.48 Construction - 8HP Standard CPU with AGP

This standard CPU configuration comprises:-

- Passively cooled base with AGP 4x Radeon R7000-based graphics, dual Fast Ethernet, three USB 2.0 interfaces, combined PS-2 mouse / keyboard, COM1 and COM2 interfaces. Behind the extended front-panel is a platform for any IDE HD or Flash device with additional interfacing for FD and LPT - refer to Appendix A for further information. The minimum airflow requirements must be matched with the selected 'processor speed, CPU damage could result otherwise !

Figure 1.48 Construction of CPU with Heat-Sink Assembly



## 1.49 Power Requirements

This CPU board is a high-performance, low-power device and, as such, requires voltage, current and power timing as defined in table 1.49 for correct operation. The Inova >70W PSUs fulfil these requirements and reference should be made to this products' data sheet and user's manual.

Table 1.49 ICP-CM Power Requirements

### Supply Voltages

Signal	Voltage	I <sub>MAX</sub>
+5V	5.0V +5%/-3%	2.5A @ 600MHz 5.2A @ 1300MHz
+3.3V	3.3V +5%/-3%	1.8A
V I/O	5.0V +5%/-3% or 3.3V +5%/-3%	0.5A

### Power Dissipation

Frequency	P <sub>TOT</sub> (Typ.)	P <sub>TOT</sub> (Max.)
600MHz	13.7W	17.5W
1300MHz	19.5W	31.3W

### Power Sequencing

This CPU needs both the 5V and 3.3V lines to be switched simultaneously within a max. allowable skew of 2ms. VI/O is assumed to be connected to either the +5V or +3.3V directly.

Symbol	t <sub>MIN</sub>	t <sub>MAX</sub>
t <sub>+5V_rising_to_+3.3V_rising</sub>	-2ms	+2ms

## 1.50 Power Consumption

The illustration provided in figure 1.50 is for reference only and serves to show the 'typical-maximum' power consumption of the ICP-CM CPU. Variations in 'processor manufacture and onboard silicon make accurate testing impossible and hence, the figures shown in this illustration are subject to fluctuation.

**Note:**

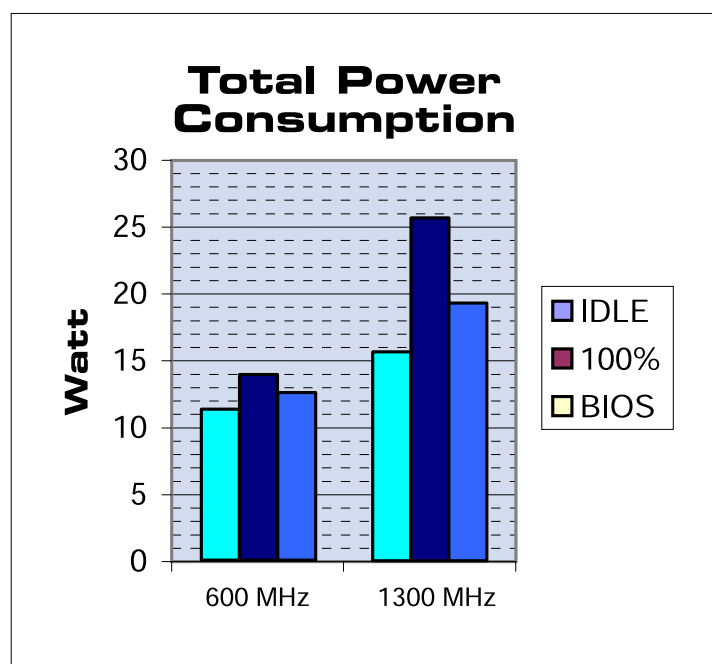
*There is no such thing as a typical application and so, the CPU power consumption was measured with the 'processor in idle state, in BIOS mode (i.e. the OS power management features were not being utilised) and software stressed to 100%*

To stress this CPU, the following software was installed:

- ▶ Microsoft Windows XP SP1,
- ▶ DirectX 9.0b,
- ▶ ATI Catalyst 3.9 video driver

on a 20GByte HD mounted on the baseboard (8HP with HD carrier) with 256Mbyte PC2100 memory and including the Radeon R7000 AGP piggyback with 32MByte video memory.

Figure 1.50 ICP-CM Power Consumption



## 1.51 Thermal Considerations

Being a passively-cooled design, a purpose-built, thermally optimized heat-sink is all that removes the heat from the CPU. The effective surface area of the radiator unit mounted on the single slot (4HP) CPU version is less than that of the 8HP CPU and therefore, necessitates more airflow (or air circulation) to keep it cool. As a guideline, the figures published in table 1.51 show the minimum airflow required to maintain stable operation. As the ambient temperature surrounding the CPU increases, so the airflow must increase.

Conclusions that can be drawn from this table are:

- ▶ Single-slot CPUs should not be integrated in applications where the environmental temp. exceeds 65°C
- ▶ CPUs intended for use in applications running at high operational temperatures ~ 85°C should be clocked at 600MHz. At greater speeds, the volume of air required to cool the core becomes so great that conventional cooling fans cannot be used.

Table 1.51 ICP-CM Airflow Requirements

Frequency	Ambient Air Temperature							
	≤ 55°C		≤ 65°C		≤ 75°C		≤ 85°C	
	8HP	4HP	8HP	4HP	8HP	4HP	8HP	4HP
600MHz	without forced cooling	0.15 m/s	0.4 m/s	0.5 m/s	0.5 m/s	0.6 m/s	0.75 m/s	
1300MHz	0.35 m/s	0.55 m/s	0.6 m/s	0.75 m/s				

Key:   Not recommended

**Note:**

*If the ambient temperature is greater than 50°C, systems utilizing the benefit of this Celeron M CPU cannot operate with a standard hard-disk, floppy or CD-ROM etc.*

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# Configuration

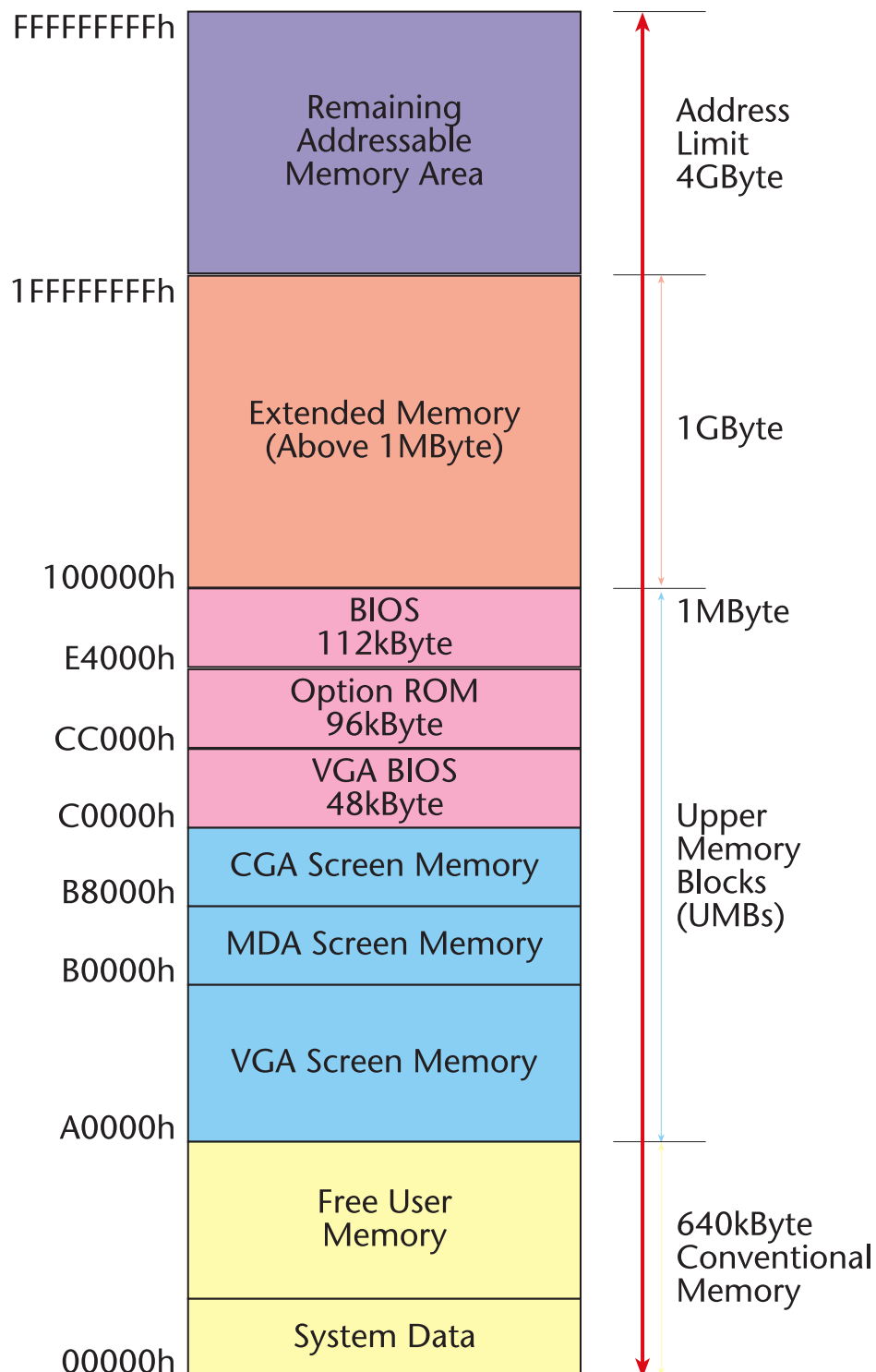
## 2

## Configuration Contents

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## 2.0 Memory Map

Figure 2.00 System Architecture



**Note:**

*96kBytes are reserved for option ROM space:*

- *USB Legacy (32kByte)*
- *Ethernet Boot (16kByte)*
- *PXE Boot (48kByte)*

*In addition, 3rd party devices can also have their 'space' here such as additional networking cards, SCSI or FireWire etc. The total available space cannot exceed 96kByte.*

## 2.1 I/O Mapped Peripherals

The original PC-XT and PC-AT desktop computer (ISA bus) specification allows for 10-bit I/O addressed peripherals. This permits peripheral boards to be I/O mapped from 0h to 3FFh. CompactPCI systems permit the full 16-bit addressing capability of the Intel 80x86 'processors, from 0h to 0FFFFh.

All Inova CPU boards include peripheral devices requiring I/O address space on board and hence the BIOS automatically assigns the I/O address required by peripheral boards and PCI devices at boot time based on the requirements of each device. The assigned addresses can be determined by reading the configuration address space registers using special software tools.

*Table 2.10 Legacy I/O Map (ISA Compatible)*

I/O Address	Description
\$000 - \$00F	8237 DMA controller #1
\$020 - \$021	8259 Master Interrupt Controller
\$040 - \$043	8254 Programmable Interval Timer #1
\$060	8042 Keyboard Controller
\$061	NMI Status
\$064	8042 Keyboard Controller
\$070 - \$071	CMOS RAM, NMI Mask Reg., RTC
\$080	Debug
\$081 - \$08B	Low DMA page registers
\$0A0 - \$0A1	8259 Slave Interrupt Controller
\$0C0 - \$0DF	8237 DMA Controller #2
\$0F0 - \$0FF	Coprocessor
\$170 - \$177 *)	Secondary Hard Disk Controller
\$1F0 - \$1F7 *)	Primary Hard Disk Controller
\$2F8 - \$2FF *)	Serial Port (COM2)

Table 2.10 Legacy I/O Map (ISA Compatible) Contd.

I/O Address	Description
\$376-\$377 *)	Secondary Hard Disk Controller
\$378 - \$37F *)	Parallel Port (LPT1) - Bi-Directional
\$3F0 - \$3F7 *)	Floppy Disk Controller
\$3F8 - \$3FF *)	Serial Port (COM1)
\$3F6 - \$3F7 *)	Primary Hard Disk Controller
\$481 — \$48B	DMA High Page Register
\$4D0 — \$4D1	Interrupt Unit Edge/Level Control Registers
\$778 - \$77F	LPT1 (ECP only)
\$CF8	PCI Configuration Address (DWORD Access Only)
\$CFC	PCI Configuration Data (DWORD Access Only)

**Note:**

*\*) Denotes Plug 'n' Play devices that are configured during the BIOS POST. Values shown are ISA compatible I/O addresses for reference only.*

## 2.2 Memory Mapped Peripherals

PC-AT desktop computers (ISA bus) allow 24-bit memory addressed peripherals. This decoding permits peripheral boards to be mapped in the Intel 80x86 memory map from 0h to 0FFFFFFh.

Inova's CompactPCI systems allow the full 32-bit addressing capability of the Intel Pentium 4 range of processors so that memory mapped peripheral devices may be mapped locally to the processor board at any location in the memory map not being used by other devices (e.g. system RAM.)

The BIOS automatically assigns memory addresses required by peripheral boards and PCI devices at boot time based on the requirements of each device. The assigned addresses can be determined by reading the configuration address space registers using PCI software tools.

**Note:**

*Devices not located on the CPU side of the PCI/PCI bridge are not normally accessible by DOS.*

## 2.3 Interrupt Routing

The IBM-compatible architecture includes one (PC-XT) or two (PC-AT) programmable interrupt controllers (Intel 8259A-compatible 'PICs') configured to set the priority of interrupt requests to the CPU.

In the PC-AT architecture, one PIC is programmed as the 'master' with one input (IRQ2) being the 'cascaded' interrupt from the second 'slave' PIC.

This configuration allows for a total of 15 interrupt sources to the CPU. Table 2.3 shows the interrupts with their corresponding vectors and sources as defined for AT PCs.

Table 2.30 PC-AT Interrupt Definitions

Interrupt Request	Interrupt Vector	Function/Assignment
IRQ0	08h	Timer
IRQ1	09h	Keyboard
IRQ2	0Ah	Slave 8259
IRQ3 <sup>1)</sup>	0Bh	COM 2
IRQ4 <sup>1)</sup>	0Ch	COM 1
IRQ5 <sup>1)</sup>	0Dh	Free for PCI
IRQ6	0Eh	Floppy
IRQ7 <sup>1)</sup>	0Fh	LPT1
IRQ8	70h	Real-Time Clock
IRQ9 <sup>1)</sup>	71h	Free for PCI
IRQ10	72h	Free for PCI
IRQ11 <sup>1)</sup>	73h	Free for PCI
IRQ12	74h	Mouse
IRQ13	75h	Co-processor
IRQ14 <sup>1)</sup>	76h	Hard Disk (IDE 0)
IRQ15 <sup>1)</sup>	77h	Hard Disk (IDE 1)

<sup>1)</sup> Entries may be reserved for ISA devices with the BIOS

## 2.4 DMA Channel Descriptions

The ICP-CM CPU can access the devices shown in table 2.4 through the specified DMA channels.

Table 2.40 DMA Channel Description

DMA Channel	Description
0	-
1	-
2	Floppy
3	LPT1 (ECP only)

## 2.5 Inova CM SMB Devices

Table 2.50 shows the addressing of the SMB (System Management Bus) Devices

*Table 2.50 SMB Devices*

Address b[7:1]	Device
0101 100	LM87 (Temperature Monitor)
1010 000	EEPROM SPD DDR Bank 0
1010 101	EEPROM TOP EXTENSION (e.g. ICP-HD-3) ID
1010 110	EEPROM RIO PANEL ID
1010 111	EEPROM Vital Product Data / General Purpose
1101 001	ICS952001 (Timing Hub)



## 2.6 Inova CM PCI Device List

Table 2.60 shows the available PCI devices both on-board and off-board (CompactPCI backplane). It should be noted that the interrupt routing assumes a standard Inova backplane configuration with a right-hand system slot.

Table 2.60 Legacy I/O Map (ISA Compatible)

Bus No.	Device Number	Function Number	IRQ	Device / Vendor ID	Description
0	0x00	0x00	N/A	0651 1039	SiS651 Host Bridge
0	0x01	0x00	N/A	0001 1039	SiS651 Virtual PPB
0	0x02	0x00	N/A	0008 1039	SiS962 LPC
0	0x03	0x00	N/A	7001 1039	SiS962 USB0 OHCI
0	0x03	0x01	N/A	7001 1039	SiS962 USB1 OHCI
0	0x03	0x02	N/A	7001 1039	SiS962 USB2 OHCI
0	0x03	0x03	N/A	7002 1039	SiS962 USB0 EHCI
0	0x02	0x05	N/A	5518 1039	SiS962 IDE
0	0x02	0x07	N/A	7012 1039	SiS962 B/S Audio
0	0x04	0x00	N/A	0900 1039	SiS962 LAN
0	0x08	0x00	INTA#	0020 3388	PCI-PCI Bridge
0	0x09	0x00	INTB#	1229 8086	LAN 82551 (Fast Ethernet)
1	0x00	0x00	INTA#	6325 1039	AGP
2	0x09		INTB#		CompactPCI Slot 8 <sup>1)</sup>
2	0x0A		INTC#		CompactPCI Slot 7
2	0x0B		INTD#		CompactPCI Slot 6
2	0x0C		INTA#		CompactPCI Slot 5
2	0x0D		INTB#		CompactPCI Slot 4
2	0x0E		INTC#		CompactPCI Slot 3
2	0x0F		INTD#		CompactPCI Slot 2 [next to Master]

Bus No. 0 = On board; Bus No. 1 = AGP; Bus No. 2 = CompactPCI Bus

<sup>1)</sup> CompactPCI backplane numeration is based on a 7-slot backplane and refers to the logical (and not physical) slot number

## 2.7 Interrupt Configuration

The CompactPCI specification defines a total of six interrupt signals on the backplane. INTA# through INTD# are used to route interrupts from the CompactPCI boards to the PIC on the 'processor board. The interrupt request level generated by the device depends on the backplane slot number which the board is plugged into, and the interrupt signal which is driven by the particular PCI device.

**Note:**

*CompactPCI interrupts may be shared by multiple sources*

Table 2.70 CompactPCI Bus Interrupts

CompactPCI Bus Interrupts	
INTA#	
INTB#	
INTC#	
INTD#	
INTP	( IRQ14 )
INTS	(IRQ15) or Serialized Interrupt - Refer to BIOS Documentation
ENUM#	Routed by BIOS

**Note:**

*Interrupts INTA through INTS and ENUM are System Master CPU inputs. INTA and ENUM are outputs if the CPU is in Peripheral Mode.*

## 2.8 Timer / Counter

The IBM-compatible architecture configures the programmable timer / counter (Intel 8254-compatible) devices for system-specific functions as shown in Table 2.80.

The BIOS programs Timer 0 to generate an interrupt approximately every 55ms (18.2 times per second.) This interrupt, known as the system timer tick, updates the BIOS clock and turns off the floppy disk motor drive after a few seconds of inactivity for example.

The BIOS featured in Inova's CPUs programs the system timer tick for PC compatibility. The interrupt generated by the timer creates an interrupt request on IRQ0 of the programmable interrupt controller (PIC) which is serviced by the CPU as interrupt vector 08h.

In addition, Timer 1 and Timer 2 are also initialised by the BIOS as necessary for the specific 'processor board functions.

Table 2.80 Timer and Counter Functions

Timer	Function/Assignment
Timer 0	System Timer, Periodic Interrupt (55 ms)
Timer 1	SDRAM Refresh
Timer 2	Speaker Frequency Generator

## 2.9 Watchdog

Two independent watchdog timers are implemented in the ICP-CM. The first timer, residing in the SiS962 South-Bridge, has a range from 4ms to 255 hours and can issue either a Reset or SMI (System Management Interrupt) upon expiry. The second timer in the Super I/O controller ranges from 1 minute to 255 minutes and issues either a Reset, IRQ or SMI upon timeout.

**Note:**

*An OS-specific driver is required to configure the watchdog timer. Please refer to the Inova WWW support pages (<http://www.inova-computers.de/web/support/public/index.html>) for the latest versions or contact Inova hotline support directly for advice .*

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# Interfaces

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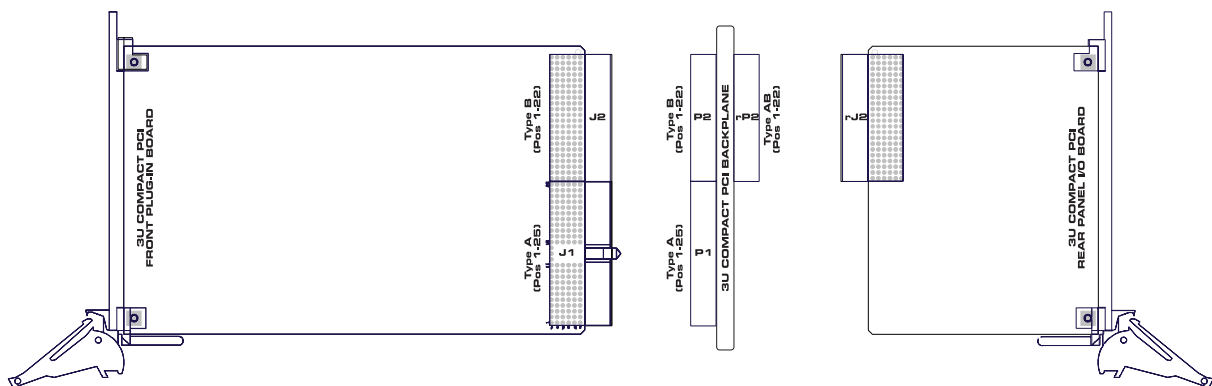
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## 3.0 CompactPCI J1/J2 Connectors

The CompactPCI standard is electrically identical to the PCI local bus standard but has been enhanced to support rugged industrial environments and up to 8 slots. The standard is based upon a 3U board size and uses a rugged pin-in-socket hard 2mm connector (IEC-1076-4-101.)

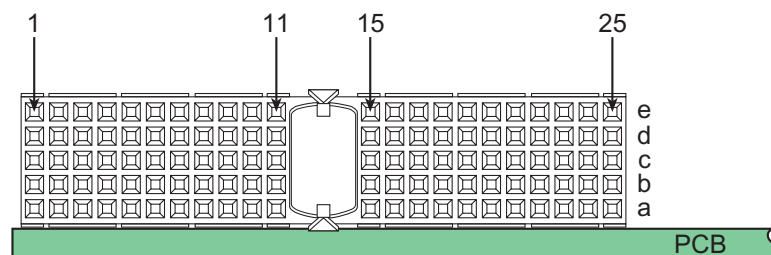
### 3.01 CompactPCI Connector Naming

Figure 3.01 Naming Convention as per PICMG 2.0 R3.0 Specification



### 3.02 CompactPCI J1 Connector

Figure 3.02 J1- 32-Bit CompactPCI Bus Interface Connector



### 3.03 ICP-PM Connector J1 and J2

Inova's ICP-CM CPU board has been designed as a 32-bit (or 64-bit) system slot device able to operate in either +5V or +3.3V (I/O) systems. The CompactPCI backplane connector is keyed accordingly (yellow for +3.3V and blue for +5V.)

**Note:**

*Do not remove the keys. An I/O board operating at 5.0V and keyed accordingly will cause a 3.3V configured system to fail if the keys are removed.*

Table 3.03 32-Bit CompactPCI J1 Pin Assignment

Pin Nr	Row A	Row B	Row C	Row D	Row E
J1-25	+5V	REQ64#	ENUM#	+3.3V	+5V
J1-24	AD[1]	+5V	V( I / O )	AD[0]	ACK64#
J1-23	+3.3V	AD[4]	AD[3]	+5V	AD[2]
J1-22	AD[7]	GND	+3.3V	AD[6]	AD[5]
J1-21	+3.3V	AD[9]	AD[8]	M66EN	C / BE[0]#
J1-20	AD[12]	GND	V( I / O )	AD[11]	AD[10]
J1-19	+3.3V	AD[15]	AD[14]	GND	AD[13]
J1-18	SERR#	GND	+3.3V	PAR	C / BE[1]#
J1-17	+3.3V	IPMB-SCL	IPMB-SDA	GND	PERR#
J1-16	DEVSEL#	GND	V( I / O )	STOP#	LOCK#
J1-15	+3.3V	FRAME#	IRDY#	GND	TRDY#
J1-14	KEY AREA				
J1-13					
J1-12					
J1-11	AD[18]	AD[17]	AD[16]	GND	C / BE[2]#
J1-10	AD[21]	GND	+3.3V	AD[20]	AD[19]
J1-09	C / BE[3]	GND (IDSEL)	AD[23]	GND	AD[22]
J1-08	AD[26]	GND	V( I / O )	AD[25]	AD[24]
J1-07	AD[30]	AD[29]	AD[28]	GND	AD[27]
J1-06	REQ0#	GND	+3.3V	CLK0	AD[31]
J1-05	-	-	RST#	GND	GNT0#
J1-04	UPS <sup>1)</sup>	GND	V( I / O )	INTP	INTS
J1-03	INTA#	INTB#	INTC#	+5V	INTD#
J1-02	TCK	+5V	TMS	TD0	TD1
J1-01	+5V	-	TRST#	+12V	+5V

<sup>1)</sup> Reserved for use for Inova's Uninterruptible Power Supply (UPS)

Table 3.04 32-Bit CompactPCI J2 Pin Assignment (Std. with Rear I/O (D))

Pin Nr	Row A	Row B	Row C	Row D	Row E
J2-22	(GA4)	(GA3)	(GA2)	(GA1)	(GA0)
J2-21	CLK6	GND	ETH1_TXF+	ETH1_TXF-	ATA_CS0#
J2-20	CLK5	GND	ATA_A0	GND	ATA_RST#
J2-19	GND	GND	ATA_A1	ETH1_RXF+	ETH1_RXF-
J2-18	LPT_STB# - COM1_TXD	LPT_PE FD_WRDATA# COM1_RXD	ATA_A2	GND	ATA_CS1#
J2-17	LPT_AFD# FD_DENSEL COM1_CTS	VGA_VSYNC	PRST#	REQ6#	GNT6#
J2-16	LPT_D0 FD_INDEX# COM1_RTS	LPT_ACK# FD_DR1# COM1_DCD	DEG#	GND	KB_CLK
J2-15	LPT_ERR# FD_HDSEL# COM1_DSR	GND	FAL#	REQ5#	GNT5#
J2-14	LPT_D1 FD_TRK0# COM1_DTR	LPT_SLCT FD_WGATE# COM1_RI	+5V (1.5A)	VGA_R	ATA_D0
J2-13	LPT_INIT FD_DIR# COM2_TXD	VGA_HSYNC	V(I/O)	ATA_D1	ATA_D2
J2-12	LPT_D2 FD_WP# COM2_RXD	ATA_IOW#	USB4_D+	GND	ATA_D3
J2-11	LPT_SLCTIN FD_STEP# COM2_CTS	GND	SMB_DAT	ATA_D4	ATA_D5
J2-10	LPT_D3 FD_RDATA# COM2_RTS	ATA_IOR#	USB4_D-	VGA_G	ATA_D6
J2-09	LPT_D4 FD_DSKCHG# COM2_DCD	PM_DAT	V(I/O)	ATA_D7	ATA_D8
J2-08	LPT_D5 FD_MSEN0 COM2_DSR	ATA_IRQ15	ATA_DMARQ	GND	ATA_D9



Table 3.04 32-Bit CompactPCI J2 Pin Assignment (Std. - with Rear I/O (D)) - Contd.

Pin Nr	Row A	Row B	Row C	Row D	Row E
J2-07	LPT_BUSY FD_MTR1# COM2_DTR	PM_CLK	SMB_CLK	ATA_D10	ATA_D11
J2-06	LPT_D6 FD_DRATE0 COM2_RI	KB_DAT	ATA_DMACK	VGA_B	ATA_D12
J2-05	LPT_D7 FD_MSEN1 -	64EN#	V(I/O)	ATA_D13	ATA_D14
J2-04	V(I/O)	SPEAKER <sup>4)</sup>	ATA_IORDY #	GND	ATA_D15
J2-03	CLK4	GND	GNT3#	REQ4#	GNT4#
J2-02	CLK2	CLK3	SYSEN#	GNT2#	REQ3#
J2-01	CLK1	GND	REQ1#	GNT1#	REQ2#

Table 3.05 Inova's ICP-CM Rear I/O J2 (CPU) Integration

Option	RIO(C1)	RIO(D)
VGA	No	Yes
Fast Ethernet	Intel 82551	Intel 82551
USB 1.1	Yes	Yes
PS-2 Mouse & Keyboard	Keyboard Only	Yes
2nd IDE Channel	Yes	Yes
Reset & Beeper	Yes	Yes

LPT1	Software Selectable	Software Selectable
COM1 & COM2	Software Selectable	Software Selectable
Floppy Disk (A or B)	Software Selectable	Software Selectable

One of

The rear I/O options described here do not detract from the latest PICMG 2.0 R3.0 specification.

- 1.) The VGA option in table 3.05 is from the chipset or mounted AGP piggyback - chipset video should not be used in parallel with the front I/O option. Doing could cause possible damage to the CPU board. If both front and rear VGA are required, then the AGP piggyback graphic option should be used which may also permit different video information to be displayed.
- 2.) The single channel Fast Ethernet option in table 3.05 is ETH 1 on the front-panel i.e. the dedicated Intel 82551 controller. If the rear I/O option is used then the front-panel connection must not be used. Doing so will disrupt the communication leading to spurious results.
- 3.) If the mouse, keyboard, LPT or COM ports are used in rear I/O applications then they should not be used from the front-panel. Communicating from both mouse and keyboard sources is physically possible but is not recommended! The front panel COM port connections are disabled if using the rear I/O COM port option.
- 4.) The CPU boasts a number of USB connection possibilities - one USB 2.0 is on the front-panel, one (USB 1.1) is just behind the panel for local device connection (custom), two (USB 2.0) are embedded within the hard disk carrier and a final USB (1.1) port is routed to the rear I/O panel.

**Note:**

*64-bit configurations cannot have rear I/O! Version (D) is preferred and is therefore the standard configuration. Transition modules connect to the backplane and provide the physical interfaces.*

## 3.1 CompactPCI Backplane

The form factor defined for CompactPCI boards is based upon the Eurocard industry standard. Both 3U (100 mm by 160 mm) and 6U (233 mm by 100 mm) board sizes are defined. A CompactPCI system is composed of up to eight CompactPCI cards. The CompactPCI backplane consists of one System Slot, and up to seven Peripheral Slots.

The System Slot provides arbitration, clock distribution, and reset functions for all boards on the bus. The System Slot is responsible for performing system initialization by managing each local board's IDSEL signal.

Physically, the System Slot may be located at either end of the backplane but Inova have placed theirs on the right to cater for physical expansion due to heat-sink, hard disk, extended functionality etc. The Peripheral Slots may contain simple boards, intelligent slaves, or PCI bus masters.

**Note:**

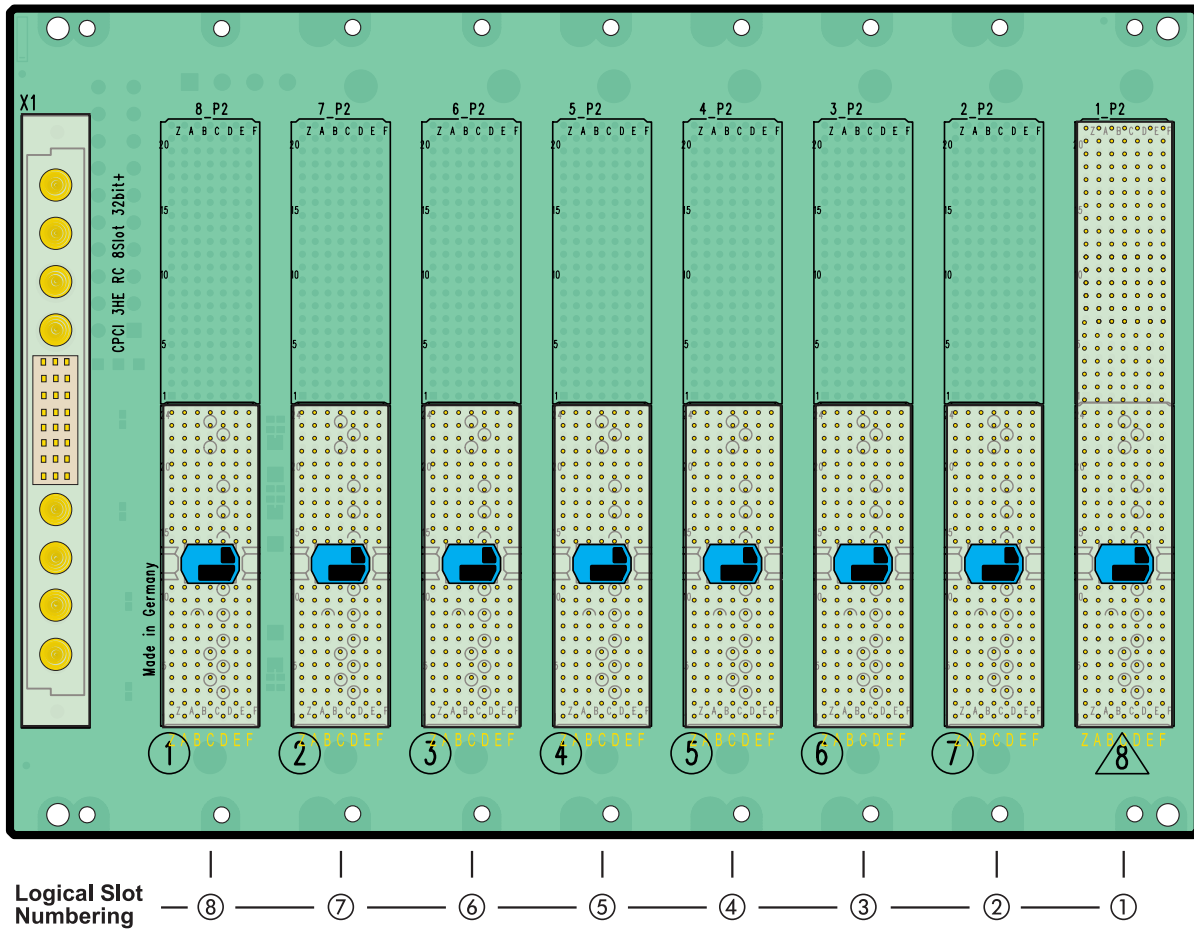
*Inova's 3U CompactPCI Celeron M CPU boards can be used as either master or slave boards i.e. occupying either the system slot or the peripheral slot. The PCI / PCI bridge automatically detects the CPU location within a system.*

**Note:**

*Older backplane revisions (rev. 2.11) cannot be used with Inova CPUs configured for rear I/O (D). Attempting to do so will cause the boot sequence to fail.*

*When installing the CPU in environments where PXI peripheral boards are being used, CPU versions without rear I/O must be used. Otherwise, signal conflict will occur on the J2 interface.*

Figure 3.10 Inova's 32-Bit CompactPCI 8-Slot Backplane - RH System Slot



**Note:**

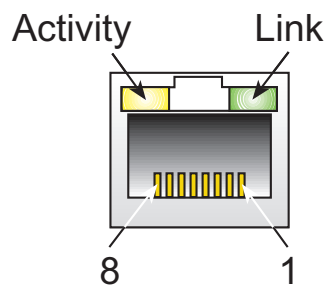
*The logical slots are different to the physical slots. The slot marked with the '△' is the System Slot and always assigned logical '1'. The neighbouring slot is logical '2'!*

## 3.2 Interfaces

### 3.2.1 J6 & J7 Ethernet

J6 is a Fast Ethernet interface from the SiS chipset while J7 [ETH1] is an additional Fast Ethernet from the dedicated on-board controller. Both RJ45 interfaces are available as standard on the CPU front-panel and provide support for 10BaseT and 100BaseTX twisted pair standards.

Figure 3.21 RJ45 Pinout



**Note:**

*Users taking advantage of the CPU's rear I/O options are advised not to use the front-panel interface [ETH1] if the rear interface is being used. Possible damage to the board could occur and data integrity cannot be assured.*

Table 3.21 Ethernet Standards & Connector Signals

Standard	Data Rate	Cable	Max. Length
IEEE802.3 10Base-T Ethernet	10Mbit/2	2-pair Cat-5	100m
IEEE802.3u 100Base-Tx Fast Ethernet	100Mbit/s	2-pair Cat-5	100m

Pin No.	Signal Description Ethernet / Fast Ethernet
1	TX0+
2	TX0-
3	RX0+
4	
5	
6	RX0-
7	
8	

## 3.22 J17 VGA Interface

J17 is available on the CPU front-panel if this option is required and if this position is not already occupied by an AGP piggyback for Panellink (TFT) or GigaST★R communication. The 15-pin high-density D-Sub connector forms the physical interface for the video on the ICP-CM which is integrated within the chipset.

The amount of graphic memory allocated to the chipset video option is defined in BIOS. Vesa resolutions up to 2048 x 1536 pixels with 32-bit colour depth are supported. Hence the full VGA, SVGA, XGA, SXGA, UXGA, HDTV and QXGA scales are covered.

## 3.23 Graphic Features (Chipset)

Table 3.23a highlights just some of the features of the standard integrated video controller.

Feature	Description
Video Accelerator	Supports single video windows with overlay function
	Supports RGB555, RGB565, YUV422, and YUV420 video formats
	Supports DVD sub-picture playback overlay
	2x 120x128 video playback line buffers to support 1920x1080 video
	Supports Direct Draw Drivers
High Integration	Built-in 64x128 CRT FIFOs to support ultra high res. graphics
	Programmable 24-bit true-colour RAMDAC up to 333MHz pixel clk
	MPEG II video playback
	Built-in TV encoder interface
Resolution, Colour & Frame Rate	Supports 333MHz clock
	Supports VESA standard super high resolution graphics modes
	Supports low-resolution modes (320x240, 512x384, 400x300)
Power Management	Supports VESA Display Power Management Signalling
	Supports clock throttling for 2D engine and 3D engine
Multimedia Application	Supports RAMDAC snoop for multimedia applications

Figure 3.23 High-Density D-Sub VGA Interface Pinout

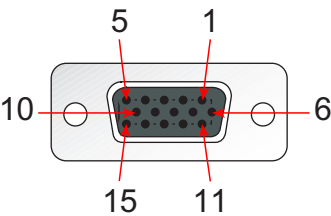


Table 3.23b Video Output Connector Signals

Pin No.	Signal
1	Analog RED
2	Analog GREEN
3	Analog BLUE
4	N/C
5, 6, 7, 8	CRT Ground
9	+5V (DDC)
10	CRT Ground
11	N/C
12	DDC-SDA
13	HSYNC
14	VSYNC
15	DDC-SCL

## 3.24 J19 USB Interface

J19 is located as standard on the front panel. All standard USB 2.0 and 1.1 compatible devices can be connected to this interface.

Figure 3.24 USB Interface Pinout

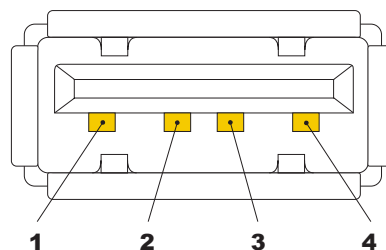


Table 3.24 USB Connector Signals

Pin No.	Signal
1	+5V
2	USB P0-
3	USB P0+
4	GND



### **3.25 J10 Hot-Swap Interface**

This PCB-level interface is used for the front-panel integrated micro-switch and blue LED in accordance with the PICMG 2.1 R2.0 specifications.

### **3.26 SW1 Reset Button**

The reset button allows the CPU to be reset in the event that it 'hangs'. Performing a reset in this manner is known as a 'warm' start as power is not removed from the peripherals (IDE etc.)

### **3.27 J9 CompactFlash Interface**

CompactFlash™ cards are designed with flash technology, a nonvolatile storage solution that does not require a battery to retain data indefinitely. CompactFlash storage cards are solid state, meaning they contain no moving parts and their low power consumption means that they consume only five percent the power required by small disk drives.

J9 is the standard CompactFlash interface and needs no further explanation.

### **3.28 Connecting the CM to the Inova ICP-HD3(-ND)**

Appendix A provides more information on the ICP-HD3(-ND) and its derivatives. For the sake of completeness however, the ICP-HD3(-ND) must only be attached / detached to / from the CM base board without power applied i.e. with the CPU removed from the CompactPCI environment. Since there aren't any flat-band cables or similar, installation is remarkably simple. The whole module plugs into the mating J12, J13 and J14 connectors.

### **3.29 Connecting the CM to the Inova IPB-FPE12**

Appendix B provides more detailed information on the IPB-FPE12 module. However, for the sake of completeness, the IPB-FPE12 connects directly to the ICP-HD3(-ND) module via a flex-cable. There isn't a direct connection possibility on the CPU base board itself.

### **3.30 Connecting the CM to a Slim-Line Floppy-Disk**

Slim-line floppy disks connect directly to the ICP-HD3(-ND) via the standard header.

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# ICP-HD-3

## ICP-HD-3 Contents

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**A**

## **A1 ICP-HD-3(-ND) CPU Extension**

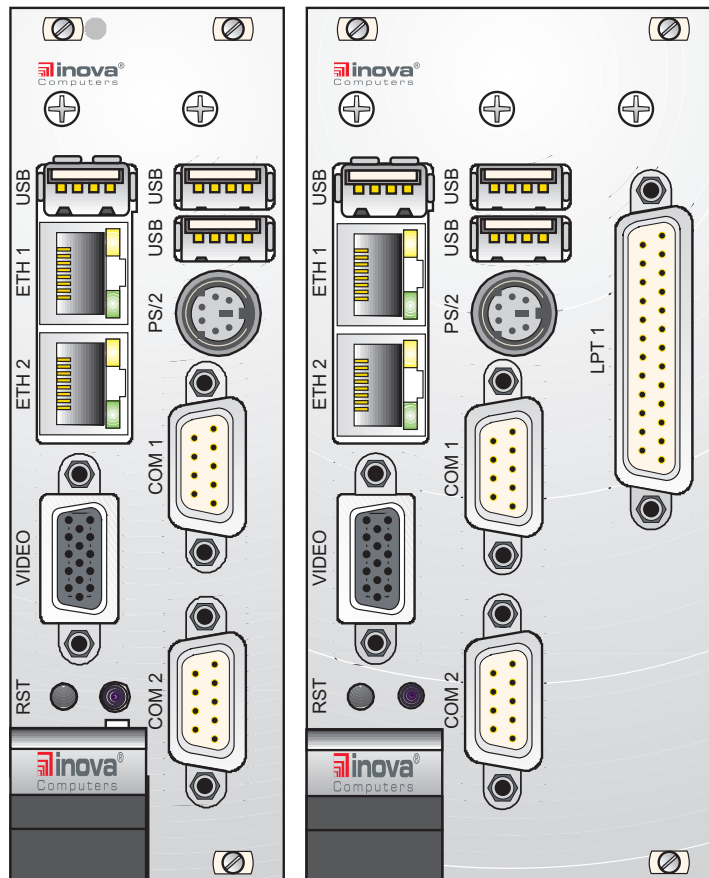
Combined PS-2 mouse / keyboard, USB (2.0), COM ports, LPT, mass storage and slim-line FD interfaces are supplied on the ICP-HD-3(-ND) - a CPU add-on board. Two versions exist - one is supplied with a hard disk and one without. Both versions are functionally identical. The name extension '-ND' refers to the No Disk version!

All communication between the ICP-HD-3 and the host CPU is performed via rigid board connectors - there aren't any flex cables on the CPU board itself! This concept eliminates the risk of incorrect device installation and ensures both mechanical and electrical stability.

### **A1.1 ICP-HD-3(-ND) Front-Panels (8HP or 12HP)**

The Inova ICP-HD-3(-ND) interface is a mass-storage carrier board that is only available as a CPU plug-in device with either an 8HP or 12HP front-panel as illustrated in figure A1.1.

*Figure A1.1 ICP-HD-3(-ND) CPU Front-Panels*



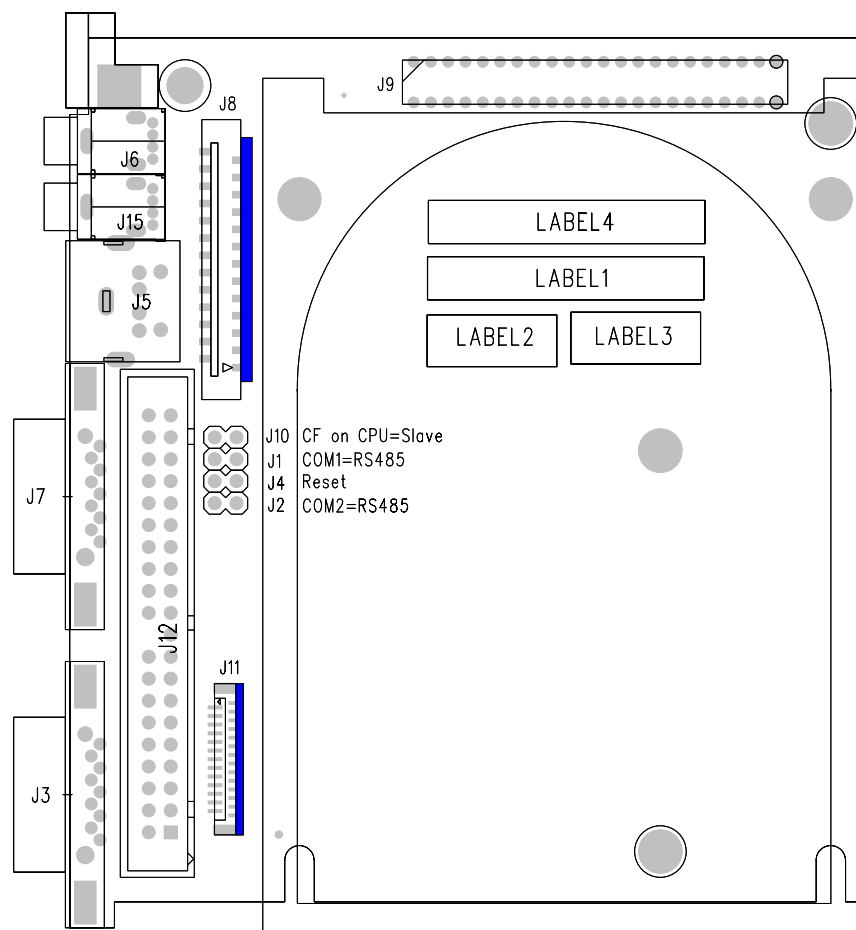
## A1.2 IDE Carrier Board ICP-HD-3(-ND)

Figure A1.2 illustrates the construction of the integrated ICP-HD-3 carrier board and the location of the interface connectors. Table A1.2 gives a description of these interfaces. Care should be exercised when attaching the LPT interface to this carrier board. Here the connection is via a length of flex cable between J11 of the carrier and J13 on the LPT module.

**Note:**  
*Damage to the CPU, hard-disk carrier board or the LPT piggyback may result if the flex cable is positioned incorrectly. Inova will not accept responsibility for negligent actions!*

*Position the blue side of the flex-cable to the blue-flanked connector shown below*

Figure A1.2 Interface Location of the ICP-HD-3(-ND) Module



A

Table A1.2 Interface Description of the ICP-HD-3(-ND) Module

Connector	Description
J1	Open: COM1 is configured for RS232 communication
	Closed: COM1 is configured for RS485 communication
J2	Open: COM2 is configured for RS232 communication
	Closed: COM2 is configured for RS485 communication
J3	COM2 physical interface
J4	Reset - shorting these pins causes the CPU to reset
J5	PS-2 mouse & keyboard physical interface
J6	USB 2.0 physical interface - USB2
J7	COM1 physical interface
J8	Slim-line floppy disk interface
J9	Notebook style 2.5" IDE header for HD or Flash etc.
J10	Open: The CompactFlash on the CPU is Master
	Closed: The CompactFlash on the CPU is Slave
J11	Flex cable interface for LPT1 (IPB-FPE12) module
J12	Standard 3.5" EIDE interface <a href="#">[80-strand cable only!]</a>
J15	USB 2.0 physical interface - USB3

The accessibility / maintainability of the mounted hard disk is ensured through the two fixing screw cutouts on the carrier board. A mounted hard disk is thus unable to shift or become dislodged in any direction.

**Note:**

*Any notebook-style IDE hard disk, Flash device or similar mass-storage unit can be connected here. However, Inova recommend only those devices from known manufacturers.*

*Connecting devices to both J9 and J12 simultaneously is not recommended. A better configuration is to use Master and Slave devices connected to J12 only or use the Rear I/O feature.*

## A2 ICP-HD-3(-ND) Interfaces

The carrier board serves not just to mount an IDE mass-storage device - it also provides the user with a wealth of familiar standard PC interfaces.

### A2.1 COM1 & COM2 Interfaces

The two COM ports feature a complete set of handshaking and modem control signals, maskable interrupt generation and highspeed data transfer rates. The selection between the RS232 and RS485 serial data communication standard is performed via J1 & J2 (COM1, COM2) illustrated in Figure A1.2.

**Note:**

*If the COM ports are used in rear I/O applications then they should not be used from the CPU front-panel. The front panel COM port connections are disabled automatically if using the rear I/O COM port option.*

Figure A2.1 COM1 & COM2 Interface Pinout

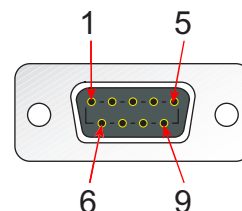


Table A2.1 COM1 & COM2 Connector Signals

Pin No.	Signal	
	RS232	RS485
1	DCD	
2	RxD	RxD, TxD +
3	TxD	RxD, TxD -
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	RI	

**Note:**

*The standard CPU configuration has both COM ports set for RS232 communication.*

*However, this device can be configured to observe a two-wire, non galvanically separated, RS485 protocol. The data direction is governed by controlling the UART's RTS signal.*

## A2.2 Mouse & Keyboard Interfaces

The physical PS-2 mouse & keyboard interface is brought out on this 8HP front-panel. Connector pinout and description are provided in Figure A2.2 and Table A2.2 respectively.

**Note:**

*If the mouse and keyboard ports are used in rear I/O applications then they should not be used from the front-panel. Communicating from both mouse and keyboard sources is physically possible but is not recommended!*

Figure A2.2 Mouse & Keyboard Interface Pinout

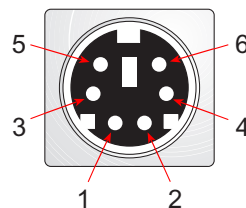


Table A2.2 Mouse & Keyboard Connector Signals

Pin No.	Signal	Pin No.	Signal
1	Data - Keyboard	2	Data - Mouse
3	GND	4	+5V
5	Clock - Keyboard	6	Clock - Mouse



## A2.3 USB 2.0 Interfaces

Standard to all ICP-HD-3 carrier board modules are the two USB (2.0) interfaces which are backward compatible to USB 1.1 devices.

Figure A2.3 USB Interface Pinout

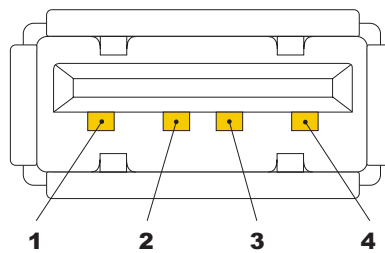


Table A2.3 USB Connector Signals

Pin No.	Signal
1	+5V
2	USB P0-
3	USB P0+
4	GND

## **A2.4 EIDE Interface**

Standard to all ICP-HD-3 carrier board modules is the 3.5" EIDE hard-disk header. This has a standard (commercial PC) pinout and requires no further mention here.

*Note:*

*To conform with the UDMA 66 (or higher) standards, only suitable, commercially available 80-strand ribbon cable should be used. Failure to do so may result in data transmission errors or even cause the CPU to crash!*

## **A2.5 Slim-Line Floppy Disk Interface**

Standard to all ICP-HD-3 carrier board modules is the slim-line floppy disk header. This has a standard (commercial PC) pinout and requires no further mention here.

# IPB-FPE12

## IPB-FPE12 Contents

**B1 IPB-FPE12 CPU Extension ..... B-2**

B1.1 J13 Interface for LPT1 ..... B-2

B1.2 IPB-FPE12 Front-Panel (4HP or 12HP) ..... B-2

*Figure B1.2 IPB-FPE12 Stand-Alone or Integrated with CPU ..... B-2*

B1.3 LPT1 Piggyback ..... B-3

*Figure B1.3 LPT1 Piggyback Board IPB-FPE12 ..... B-3*

*Table B1.3 IPB-FPE12 Connector Description ..... B-4*

B1.4 LPT1 Interface ..... B-4

*Figure B1.4 LPT1 Interface Pinout ..... B-4*

*Table B1.4 LPT1 Connector Signals ..... B-4*



## **B1 IPB-FPE12 CPU Extension**

The Inova IPB-FPE12 adds LPT functionality to any Inova Pentium M, Celeron M or Pentium 4(M) CPU. The piggyback is available as a stand-alone device with its own 4HP front-panel or integrated within a 12HP front-panel. The information documented here is valid regardless of the connection choice.

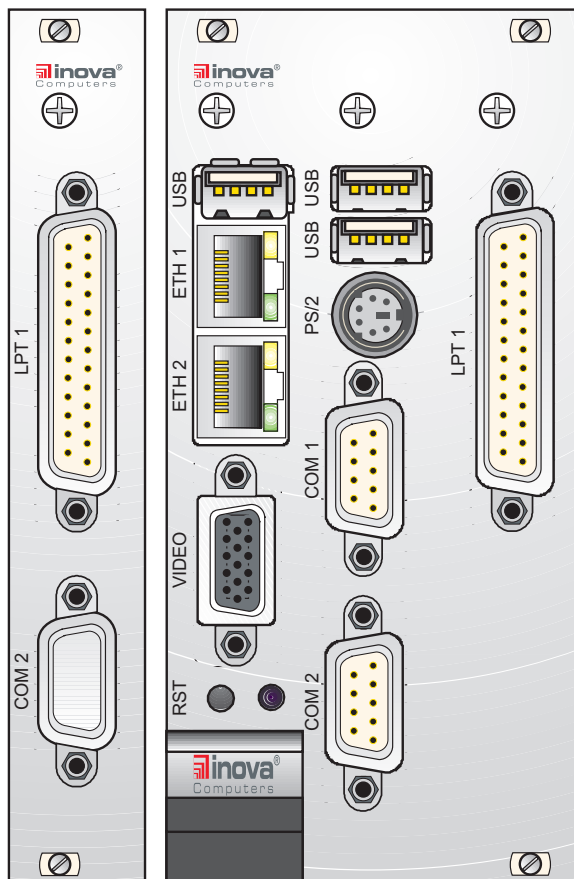
### **B1.1 J13 Interface for LPT1**

The control of the LPT interface is performed through the J11 connector on the CPU's hard-disk carrier board. The location of this connector may be determined by referring to Appendix A of this User's Manual. The flex cable connection and function of the LPT interface are discussed in this section.

### **B1.2 IPB-FPE12 Front-Panel (4HP or 12HP)**

The Inova IPB-FPE12 interface is a small piggyback available as a stand-alone device with its own 4HP front-panel or integrated with the CPU as in figure B1.2.

*Figure B1.2 IPB-FPE12 Stand-Alone or Integrated with CPU*



**Note:**  
*Although COM2 is shown on the left-hand stand-alone front-panel, this interface will not be present in the delivered module. A dust cap replaces the 9-pin D-Sub connector!*

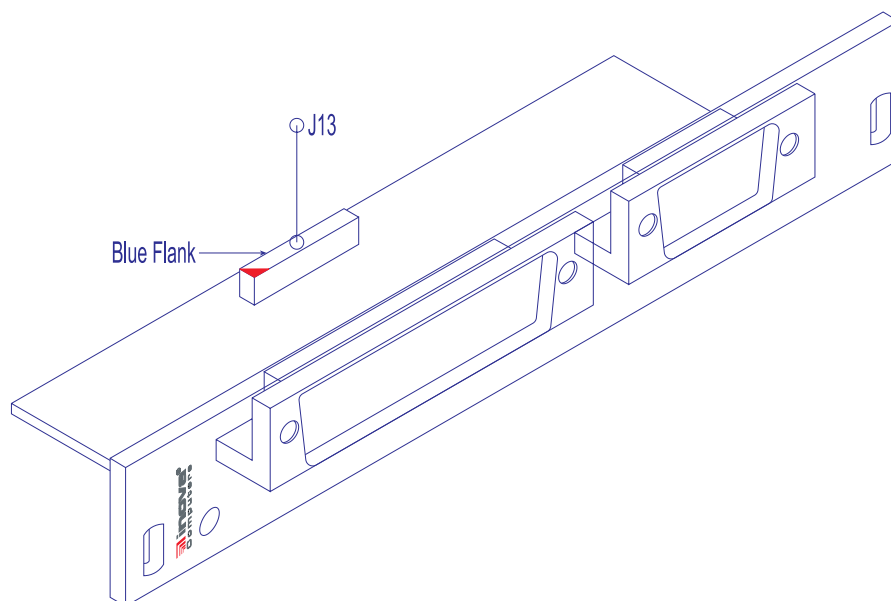
*If an LPT or slim-line FD configured to communicate via the rear I/O (RIO) transition module then the LPT interface cannot be used here. Trying to do so will result in data corruption and possible damage to the logic components*

## B1.3 LPT1 Piggyback

Figure B1.3 illustrates the construction of the stand-alone IPB-FPE12 piggyback and the upperside location of the J13 connector. The same mechanical construction applies to the integrated version. Care should be taken to ensure that pin 1 of J13 on the CPU base board is linked by an appropriate length of flex cable to pin 1 on the ICP-HD-3 piggyback. To help with the orientation, the connector flanks that are blue indicate the blue face of the flex-cable. Unmarked flanks indicate the metallic connection of the flex-cable. Also, pin 1 has been highlighted by a red triangle.

**Note:**  
*Damage to the CPU, hard-disk carrier board or the piggyback may result if the flex cable is positioned incorrectly. Inova will not accept responsibility for negligent actions!*

Figure B1.3 LPT1 Piggyback Board IPB-FPE12



**Note:**  
*The physical connection of the IPB-FPE12 is electrically identical regardless of the nature of connection (stand-alone or integrated!)*

Table B1.3 IPB-FPE12 Connector Description

Connector	Description
J13	LPT1

## B1.4 LPT1 Interface

The physical LPT1 interface is either integrated into a 12HP CPU front-panel or available as a separate 4HP unit. The piggyback located behind this interface connects to the hard-disk carrier board (ICP-HD-3) mounted J13 connector.

Figure B1.4 LPT1 Interface Pinout

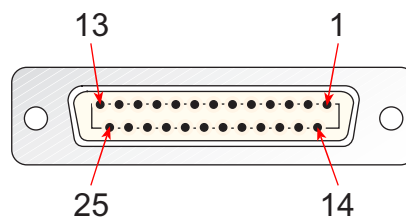


Table B1.4 LPT1 Connector Signals

Pin No.	Signal	Pin No.	Signal
1	STROBE	2	PD0
3	PD1	4	PD2
5	PD3	6	PD4
7	PD5	8	PD6
9	PD7	10	ACK
11	BUSY	12	PE
13	SLCT	14	AUTOFD
15	ERROR	16	INIT
17	SLCTIN	18-25	GND

# ITM-RIO

## ITM-RIO Contents

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Table C1.10 Valid Rear I/O Configurations .....	C-2
Table C1.11 Rear I/O Module Functionality .....	C-2
C1.2 ITM-RIO Rear-Panels (4HP or 8HP) .....	C-3
Figure C1.2 The rear Panels of the Inova ITM-RIO-D-x .....	C-3
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## C1 ITM-RIO CPU Extension

The Inova Pentium 4(M), Pentium M or Celeron M CPUs are more than just a computing platform - they are a complete, well thought-out concept. Nowhere is this more apparent than in the colourful rear I/O selection. With a choice of three full-length (80mm) plug-in modules conforming to the latest Inova rear I/O (D) specification and the rear I/O (C1) options, the major industrial requirements have been satisfied.

### C1.1 ITM-RIO-D Configurations

Rear I/O (D) is the standard configuration for the Pentium 4(M), Pentium M and Celeron M series of high-performance CPUs. Table C1.10 illustrates the configurations stemming from one single PCB layout - with backward compatibility to some of the features provided in the Inova rear I/O (C) boards. Table C1.11 shows the functionality of the 4 Inova rear I/O compatible modules.

Table C1.10 Valid Rear I/O Configurations

Option	RIO(C1)	RIO(D)
VGA	No	Yes
Fast Ethernet	See Matrix	See Matrix
USB 1.1	Yes	Yes
PS-2 Mouse & Keyboard	Keyboard Only	Yes
2nd IDE Channel	Yes	Yes
Reset & Beeper	Yes	Yes

Controller	Processor		
	P4	PM	CM
Intel	82551	82540EM	82551
SiS	900	900	900
RIO	82551	900	82551

LAN Networking Matrix

LPT1	Software Selectable	Software Selectable
COM1 & COM2	Software Selectable	Software Selectable
Floppy Disk (A or B)	Software Selectable	Software Selectable

One of

Table C1.11 Rear I/O Module Functionality

Product Name	VGA Graphic	Fast Ethernet	USB	I/O	Mouse / Keyboard	Mass Storage	Full Length
ITM-RIO-D-0	Yes	See Matrix	1.1	LPT1	Both	Header	Yes ( 80mm )
ITM-RIO-D-1	Yes	See Matrix	1.1	COM1 & COM2	Both	Header	Yes (80mm )
ITM-RIO-D-2	Yes	See Matrix	1.1	FD-A	Keyboard	Header	Yes ( 80mm )
ITM-RIO-FHLU	No	None	1.1	FD-A	No	Header	No (25mm )

All transition modules have reset and beeper pins

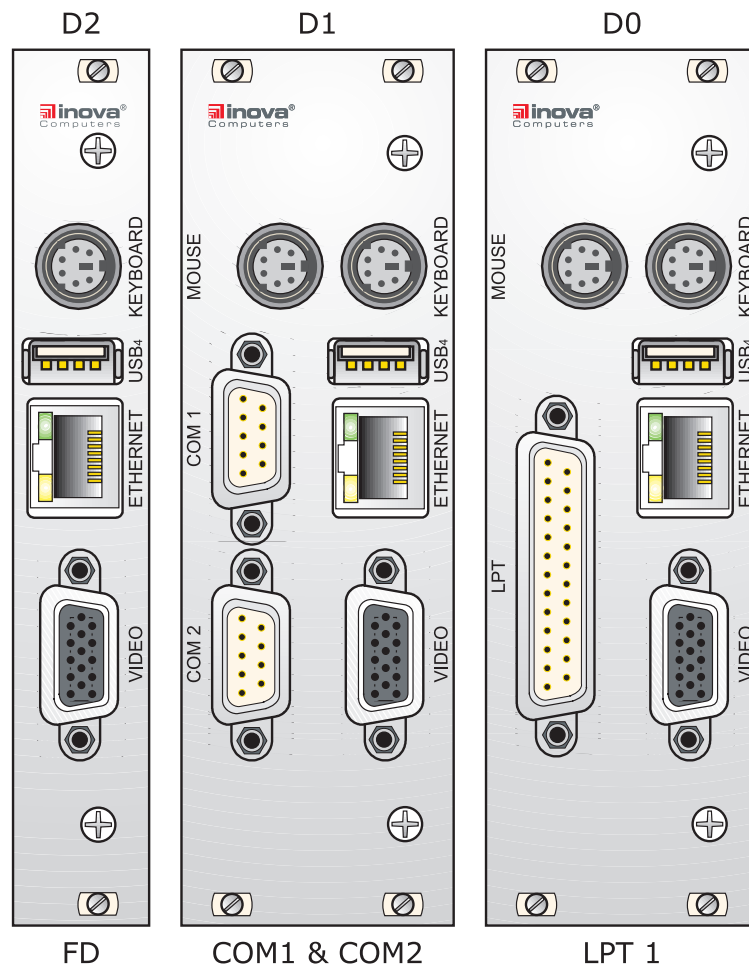
Auto-configuration RIO(D) feature can be overridden in BIOS. Settings MUST be made manually if equipped with RIO (C)



## C1.2 ITM-RIO Rear-Panels (4HP or 8HP)

As with front-panel I/O, the physical interfaces from the ITM-RIO-D-x rear I/O module are brought out to a face plate (rear panel). Figure C1.2 illustrates the three standard formats available (at time of press.)

Figure C1.2 The rear Panels of the Inova ITM-RIO-D-x



The rear I/O options described here do not detract from the latest PICMG 2.0 R3.0 specification.

The VGA option in table C1.10 can be from either the chipset or the AGP piggyback option. Using the chipset graphics for both front and rear I/O simultaneously is not advisable as the loading may be too great. If both front and rear I/O VGA are required then the twin-engined, Radeon-based AGP piggyback graphic option should be used.

The single channel Fast Ethernet option in table C1.10 is either ETH1 or ETH 2 on the front-panel depending on the computer platform. If the rear I/O option is used then the front-panel connection must not be used. Doing so will disrupt the communication leading to spurious results.

If the mouse, keyboard and COM ports are used in rear I/O applications then they should not be used from the front-panel. Communicating from both mouse and keyboard sources is physically possible but is not recommended!

### C1.3 ITM-RIO-D-x Transition Module

Figure C1.3 illustrates the construction of the ITM-RIO-D-x module. The connections are straight forward and need little by way of explanation. None of the connectors can be incorrectly inserted thanks to the mechanical keying of both plug and socket. Table C1.3 explains the significance of the interfaces labelled in Figure C1.3.

**Note:**

*Care should be exercised when inserting the cables linking the COM, LPT, EIDE and floppy etc. Only those cables supplied by Inova Computers should be used.*

Figure C1.3 Inova Rear I/O Transition Module ITM-RIO-D-x

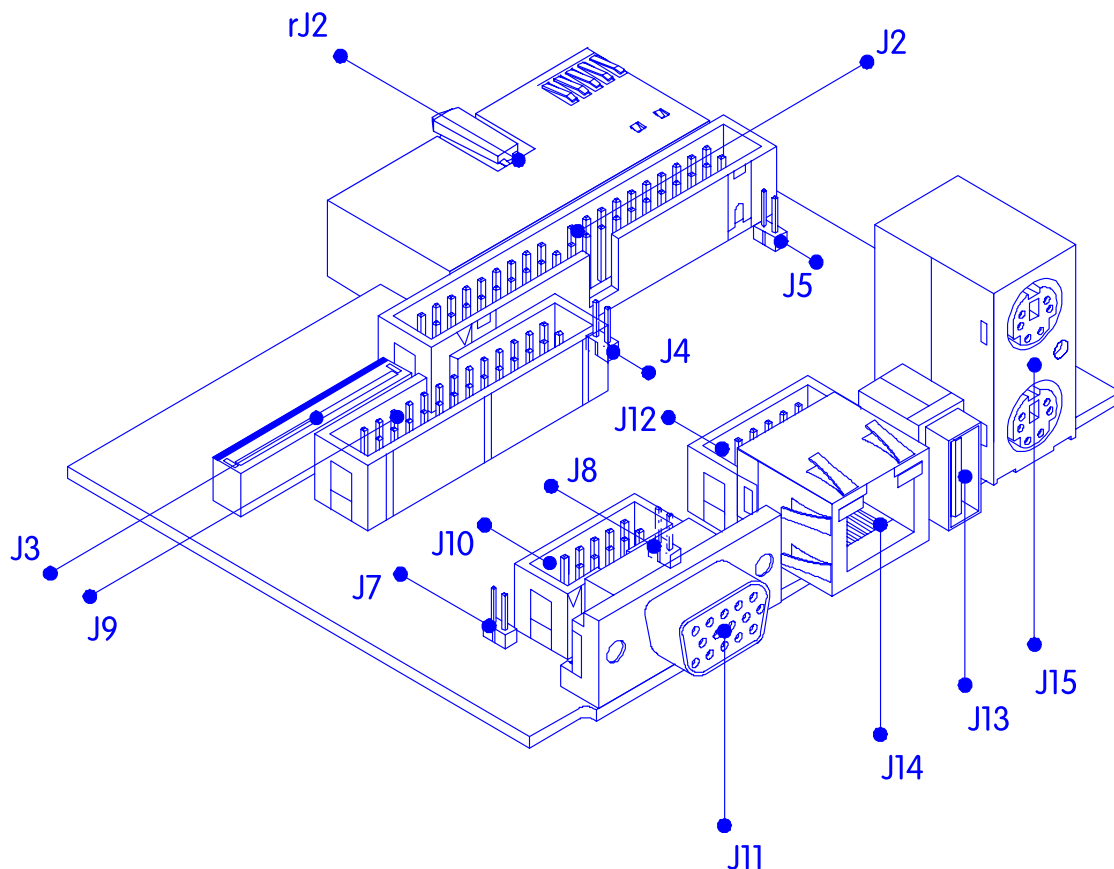


Table C1.3 ITM-RIO-D-x Connector Description

Connector	Description
J1	CompactPCI rear I/O connector
J2	Standard 3.5" IDE header
J3	Standard slim-line floppy disk interface
J4	Beeper (loudspeaker)
J5	Reset
J7	Open: COM2 is configured for RS232 communication
	Closed: COM2 is configured for RS485 communication
J8	Open: COM1 is configured for RS232 communication
	Closed: COM1 is configured for RS485 communication
J9	LPT1
J10	COM2
J11	VGA physical interface
J12	COM1
J13	USB physical interface (USB 4)
J14	Fast Ethernet physical interface
J15	PS-2 mouse & keyboard interface [only keyboard on ITM-RIO-D-2 ]

**Note:**

*When setting up the rear I/O (D) the following should be observed:*

*Either the LPT interface or the COM ports or the floppy disk interface can be used (not combined)*

*Only the required device should be attached. Installing or attaching hardware that is not required will prevent the actual device from being configured. Example: if a FD is physically attached but the COM ports are required, then these ports will not work even if they are correctly configured in BIOS!*

## C1.4 COM1 & COM2 Interfaces

The two COM ports feature a complete set of handshaking and modem control signals, maskable interrupt generation and highspeed data transfer rates. An 8HP rear-panel (Figure C1.2) brings out the physical COM1 & COM2 interfaces.

**Note:**

*If the COM ports are used in rear I/O applications then they should not be used from the CPU front-panel.*

*The front panel COM port connections are disabled automatically if using the rear I/O COM port option.*

Figure C1.4 COM1 & COM2 Interface Pinout

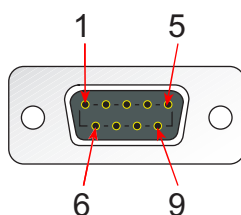


Table C1.4 COM1 & COM2 Connector Signals

Pin No.	Signal	
	RS232	RS485
1	DCD	
2	RxD	RxD, TxD +
3	TxD	RxD, TxD -
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	RI	

**Note:**

*The standard CPU configuration has both COM ports set for RS232 communication.*

*However, this device can be configured (J7 and J8) to observe a two-wire, non galvanically separated, RS485 protocol. The data direction is governed by controlling the UART's RTS signal.*

C1.5 LPT1 Interface

The physical LPT1 interface of the rear I/O panel illustrated in Figure C1.2 connects to J9 on the baseboard for.

*Note:*

*If the LPT port is used in rear I/O applications then it should not be used from the front-panel. Communicating from both sources is physically possible but is not recommended!*

Figure C1.5 LPT1 Interface Pinout

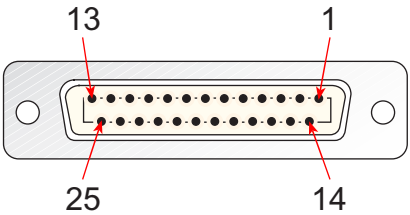


Table C1.5 LPT1 Connector Signals

Pin No.	Signal	Pin No.	Signal
1	STROBE	2	PD0
3	PD1	4	PD2
5	PD3	6	PD4
7	PD5	8	PD6
9	PD7	10	ACK
11	BUSY	12	PE
13	SLCT	14	AUTOFD
15	ERROR	16	INIT
17	SLCTIN	18-25	GND

## C1.6 Mouse & Keyboard Interfaces

The physical PS-2 keyboard interface is brought out on either a 4HP or 8HP rear -panel, the mouse interface is only available on the 8HP version (Figure C1.2) Connector pinout and description are provided in Figure C1.6 and Table C1.6 respectively.

**Note:**

*If the mouse, keyboard ports are used in rear I/O applications then they should not be used from the front-panel. Communicating from both mouse and keyboard sources is physically possible but is not recommended!*

Figure C1.6 Mouse & Keyboard Interface Pinout

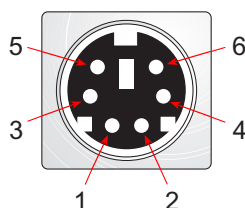


Table C1.6 Mouse & Keyboard Connector Signals

Pin No.	Signal	Pin No.	Signal
1	Data	2	N/C
3	GND	4	+5V
5	CLK	6	N/C

## C1.7 VGA Interface

The VGA signals appearing on this interface are from the CPU chipset or AGP piggyback (if configured for rear I/O signalling). Figure C1.7 and Table C1.7 provide the pinout and signal description of this standard VGA interface respectively. With an AGP video piggyback installed, the video image appearing on this rear I/O interface can be selected to be different to that appearing on the front-panel. This is possible through (in this case) the piggyback's dual independent Radeon 7000 graphics engines.

**Note:**

*Using the chipset graphics for both front and rear I/O simultaneously is not advisable as the loading may be too great. If both front and rear I/O VGA are required then the twin-engined, Radeon-based AGP piggyback graphic option should be used.*

Figure C1.7 VGA Interface Pinout

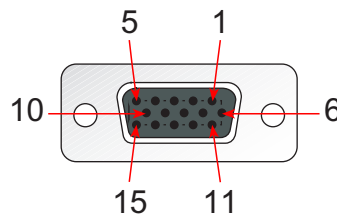


Table C1.7 Video Output Connector Signals

Pin No.	Signal
1	Analog RED
2	Analog GREEN
3	Analog BLUE
4	N/C
5, 6, 7, 8	CRT Ground
9	+5V (DDC)
10	CRT Ground
11	N/C
12	DDC-SDA
13	HSYNC
14	VSYNC
15	DDC-SCL

## C1.8 Fast Ethernet Interface

Standard to all rear I/O (D) transition modules is the Fast Ethernet connection. Figure C1.8 and Table C1.8 provide the pinout and signal description of this standard Ethernet interface respectively. Although the LEDs feature on the Ethernet connector, these are not physically connected to the rear I/O interface board. Instead, if this interface is used, communication traffic can still be observed on the front-panel Ethernet connector!

**Note:**

*The single channel Fast Ethernet option in table C1.10 is either ETH 1 or ETH 2 on the front-panel depending on the computer platform. If the rear I/O option is used then the front-panel connection using the same controller must not be used. Doing so will disrupt the communication leading to spurious results.*

Figure C1.8 Fast Ethernet Interface Pinout

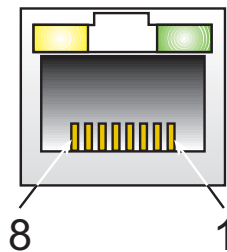


Table C1.8 Fast Ethernet Connector Signals

Pin No.	Signal Description Ethernet / Fast Ethernet
1	TX0+
2	TX0-
3	RX0+
4	
5	
6	RX0-
7	
8	



## C1.9 USB Interface (USB 4)

Standard to all rear I/O (D) transition modules is the peripheral USB (1.1) port. Figure C1.9 and Table C1.9 provide the pinout and signal description of this standard Ethernet interface respectively.

Figure C1.9 USB Interface Pinout

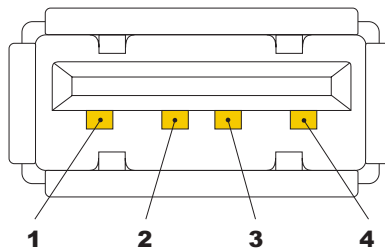


Table C1.9 USB Connector Signals

Pin No.	Signal
1	+5V
2	USB P2-
3	USB P2+
4	GND

### **C1.10 EIDE Interface**

Standard to all rear I/O transition modules is the 3.5" EIDE hard-disk header. This has a standard (commercial PC) pinout and requires no further mention here.

*Note:*

*To conform with the ATA 5 standard,  
only suitable, commercially available  
80-strand ribbon cable should be  
used. Failure to do so may result in  
data transmission errors or even cause  
the CPU to crash!*

### **C1.11 Slim-Line Floppy Disk Interface**

Standard to all rear I/O transition modules is the slim-line floppy disk header. This has a standard (commercial PC) pinout and requires no further mention here.

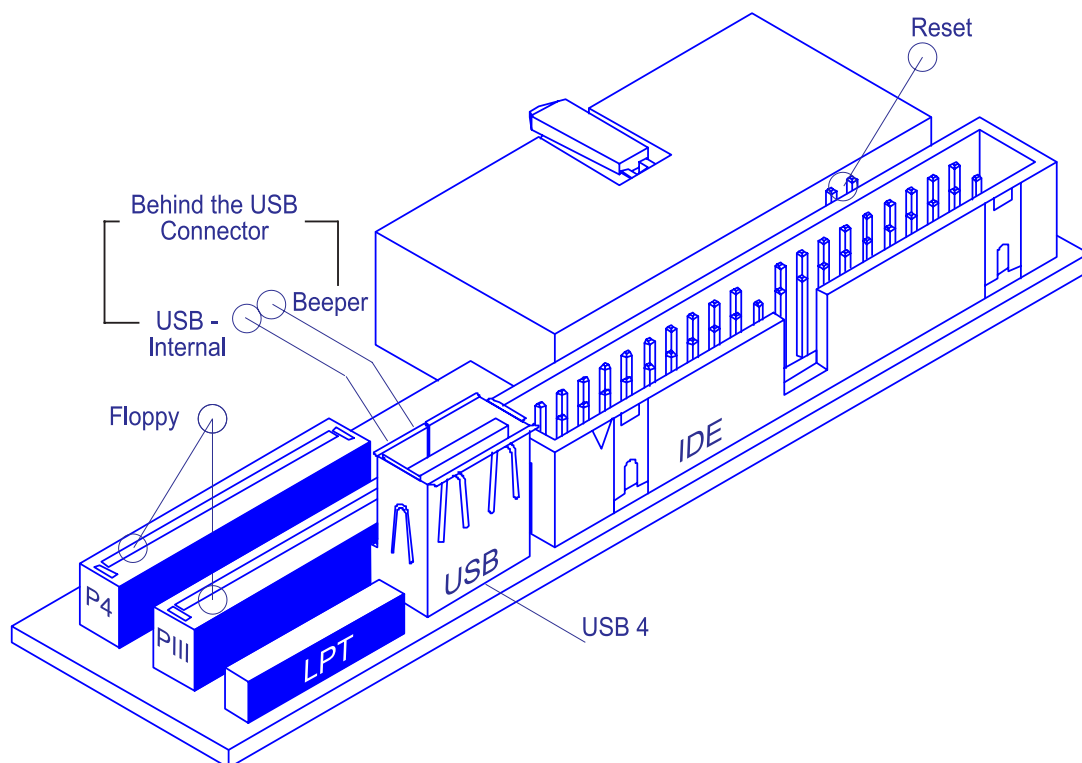
### C1.12 ITM-RIO(C&D)-FHLU Extension

To further enhance the I/O and serviceability of their CPUs, Inova have introduced a rear I/O module (figure C1.12) that connects to a CompactPCI connector on the rear of the Master Slot on the backplane. All standard Inova backplanes are equipped with this R2 connector so that even if the rear I/O functionality is not requested at time of order, it can be implemented at a later stage.

One of the advantages of this module (apart from its obvious size benefit) is its ability to attach a 3.5" IDE device (or Inova IPM-ATA Mass Storage Device) without direct connection to the CPU base board. This facilitates servicing and allows a CPU for example, to be exchanged without touching the software stored on the HD. Likewise, a hard-disk can be swapped without having to disassemble the CPU! Two slim-line (notebook) floppy interfaces are implemented allowing the module to be compatible with existing Inova PIII CPUs (with RIO(C)) as well as the P4, PM and CM family.

The integration of USB (1.1) with both the standard connector and notebook style internal connector facilitates the integration of commercially available FDs or similar devices. The signal description of the standard connector can be obtained by referring to page C - 11

Figure C1.12 ITM-RIO(C&D)-FHLU



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# IPM-ATA

## IPM-ATA

**D1 IPM-ATA CPU Extension ..... D-2**

D1.1 rj2 Interface ..... D-2

*Figure D1.1a Dedicated IPM-ATA Backplane ..... D-2*

D1.1 rj2 Interfaces (Contd.) ..... D-3

*Figure D1.1b The Complete Connection Picture ..... D-3*

D1.2 IPM-ATA-HD ..... D-4

*Figure D1.2 IPM-ATA-HD Board Layout ..... D-4*

*Table D1.2 IPM-ATA-HD Jumper Description (CF Socket) ..... D-4*

D1.3 IPM-ATA-CF ..... D-5

*Figure D1.3 IPM-ATA-CF Board Layout ..... D-5*

*Table D1.3 IPM-ATA-CF Jumper Description ..... D-5*

D1.4 IPM-ATA-PCMCIA ..... D-6

*Figure D1.4 IPM-ATA-PCMCIA Board Layout ..... D-6*

*Table D1.4 IPM-ATA-PCMCIA Jumper Description ..... D-6*

D1.5 Device Compatibility ..... D-7

*Table D1.5 Compatibility List ..... D-7*



## D1 IPM-ATA CPU Extension

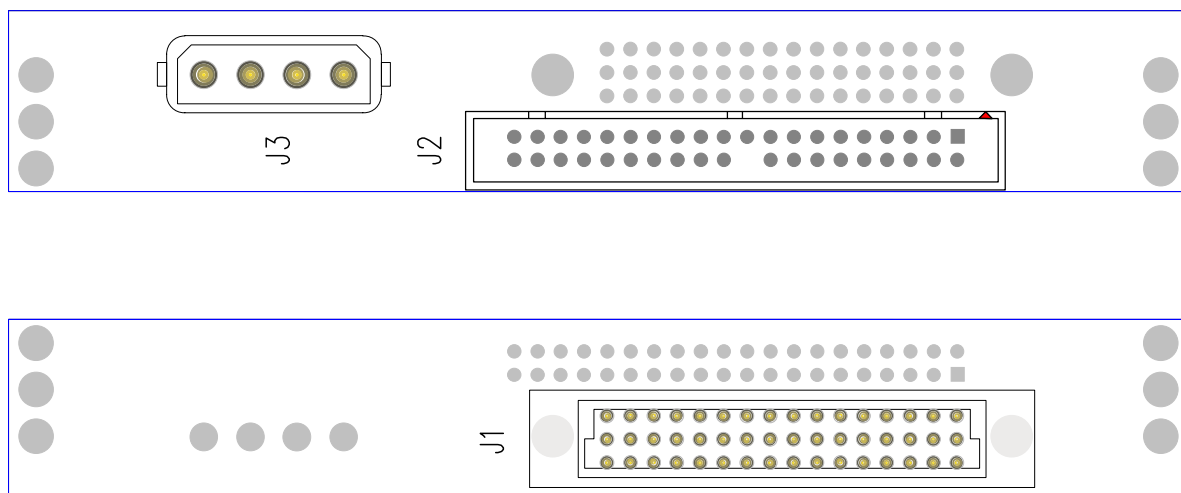
Inova Plug-In Module (IPM-) offers the user the ability to exchange a hard-disk for example without having to remove the CPU from the CompactPCI enclosure and then dismantle it etc. Currently, three units exist that provide industry with hard-disk, Compact FLASH, MicroDrive or ATA PCMCIA format mass storage capability.

### D1.1 rJ2 Interface

All IPM-ATA modules possess rJ2 for data communication between the CompactPCI backplane and the mass storage unit(s) in question. Figure D1.1a illustrates the dedicated IPM-ATA backplane and connectors.

**Note:**  
*The IPM-ATA modules can only be used in CompactPCI systems that have been prepared for rear I/O or have the IDE signals available on the rear rP2 connector that are in accordance with the specification for RIO. In addition, the rear rP2 CompactPCI connector must be present.*

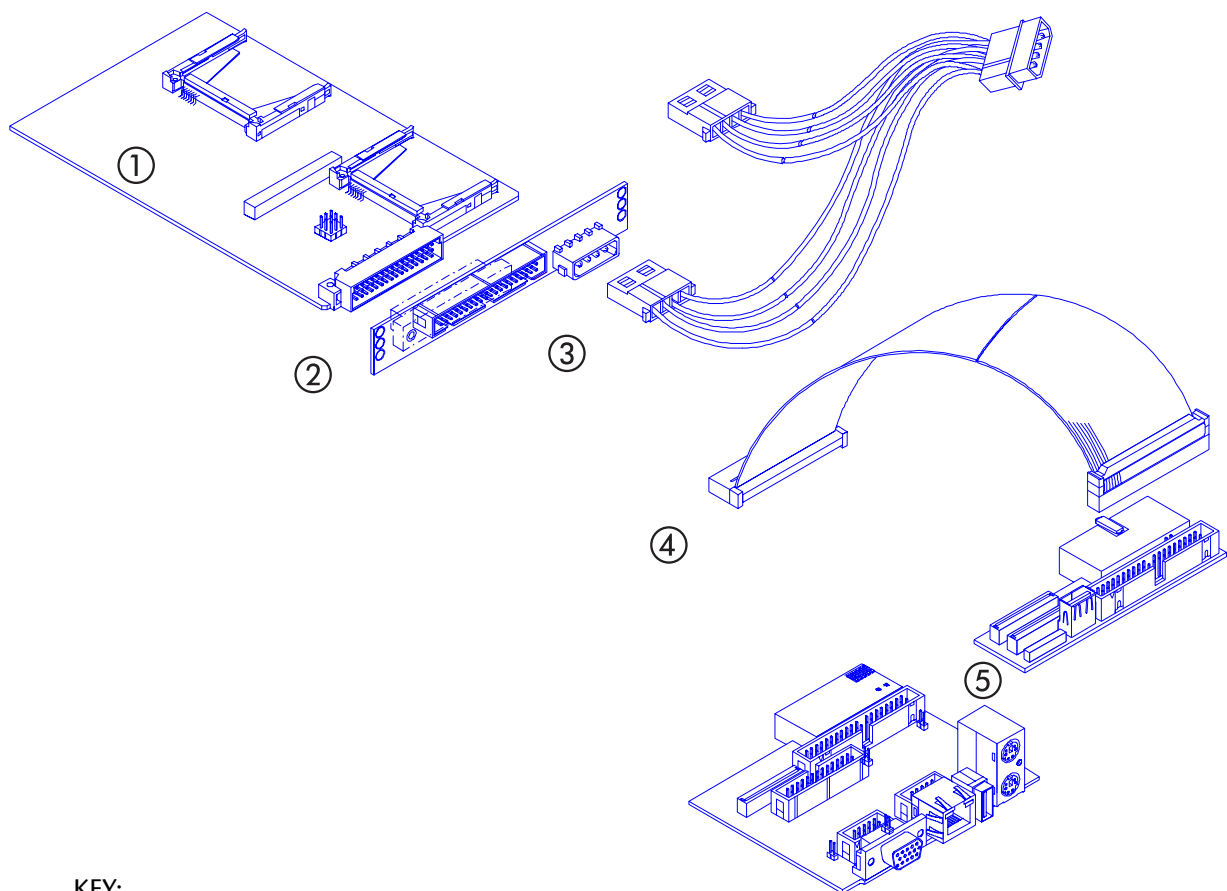
Figure D1.1a Dedicated IPM-ATA Backplane



## D1.1 rJ2 Interfaces (Contd.)

Standard 80-pin IDE ribbon-cable is used to connect rJ2 of the ITM-RIO modules to the IPM's dedicated backplane. The use of ribbon cable permits the mass-storage device(s) to be positioned at any convenient location within the CompactPCI enclosure. Figure D1.1b shows the complete configuration (CompactPCI to IPM-XXX)

Figure D1.1b The Complete Connection Picture



**KEY:**

1. IPM-ATA carrier board
2. Dedicated backplane with standard IDE header and power cord interface
3. Y-Cable for bringing the power from the CompactPCI backplane and to this and another device
4. Standard 80-strand, ATA-5 [UDMA-66 or higher] IDE ribbon cable (30cm)
5. Inova rear I/O module (ITM-RIO) with IDE connection

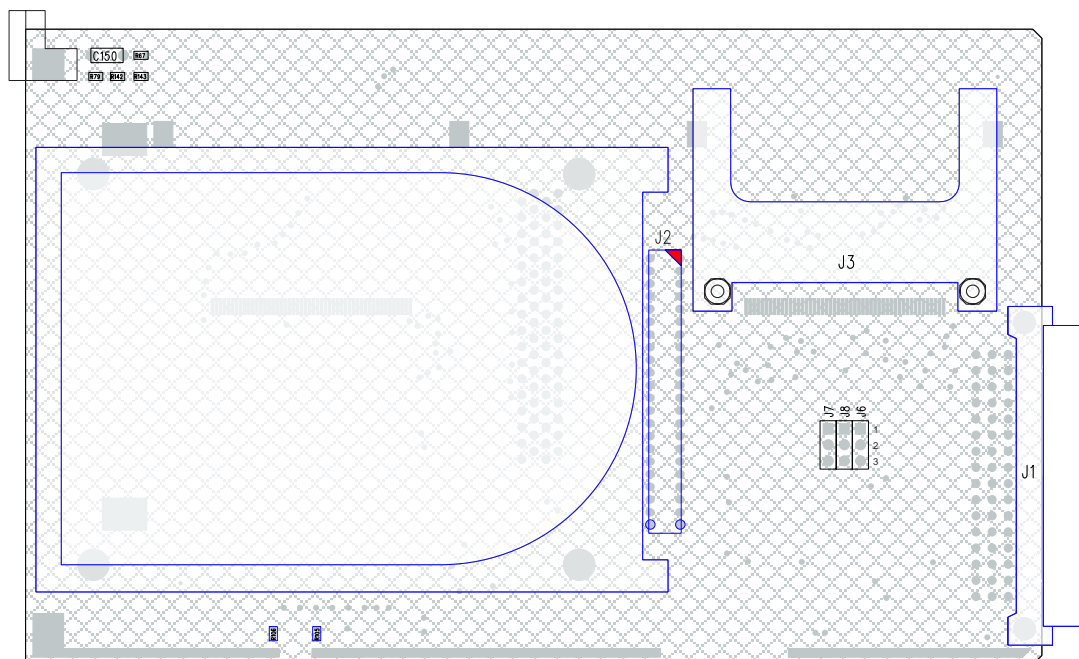
**Note:**

*The IDE cabling used should conform to at least ATA-5 standards (80-strand)*

## D1.2 IPM-ATA-HD

The IPM-ATA-HD has provision for one standard notebook (2.5") EIDE device (FLASH or hard-disk) and one Compact FLASH or MicroDrive site. Figure D1.2 illustrates the significant connectors for this device while Table D1.2 indicates the jumper positions for the various Master/Slave device configurations.

Figure D1.2 IPM-ATA-HD Board Layout



**Note:**

*The hard disk is jumpered seperately for Master / Slave operation*

Table D1.2 IPM-ATA-HD Jumper Description (CF Socket)

Jumper J6	CompactFlash or MicroDrive in J3
2-3	Master
Open	Slave

It should be noted that the secondary IDE channel (from rear I/O) only is available for use by the IPM-ATA-HD (the primary is on the CPU board itself). Multi Master or multi Slave configurations are not supported and will not work!



D1.3 IPM-ATA-CF

The IPM-ATA-CF has provision for one or two standard Compact FLASH or MicroDrive devices. Figure D1.3 illustrates the significant connectors for this device while Table D1.3 indicates the jumper settings for the various Master/Slave device configurations.

Figure D1.3 IPM-ATA-CF Board Layout

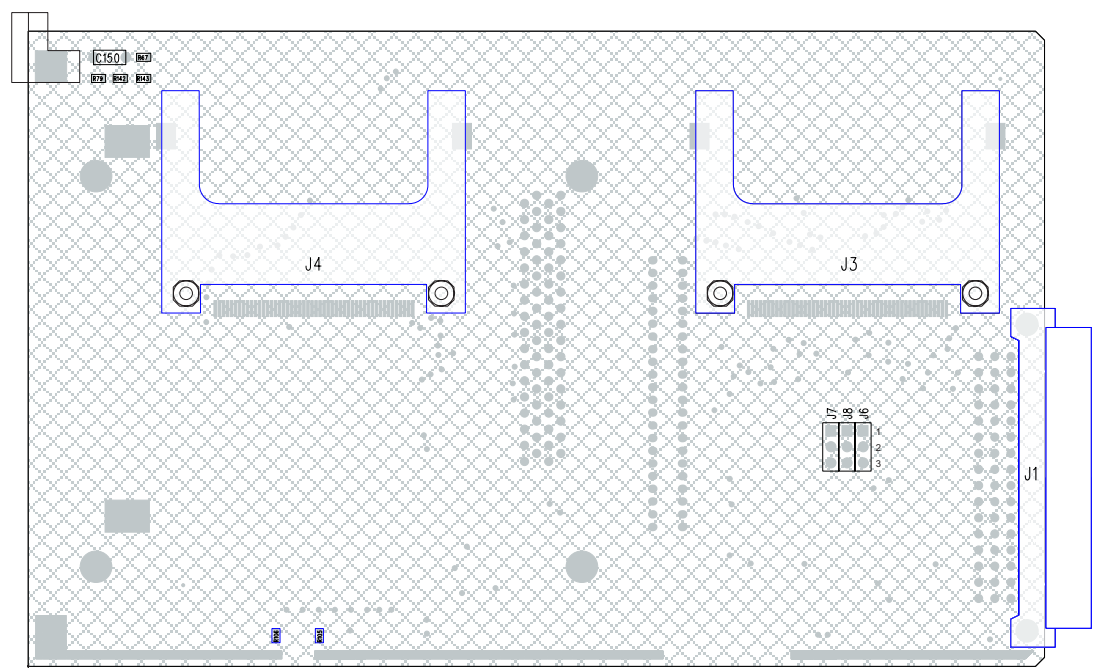


Table D1.3 IPM-ATA-CF Jumper Description

Jumper J6	CompactFlash or MicroDrive in J3	Jumper J7	CompactFlash or MicroDrive in J4
2-3	Master	2-3	Master
Open	Slave	Open	Slave

It should be noted that the secondary IDE channel only (from rear I/O) is available for use by the IPM-ATA-CF (the primary is on the CPU board itself). Multi Master or multi Slave configurations are not supported and will not work!

## D1.4 IPM-ATA-PCMCIA

The IPM-ATA-PCMCIA has provision for one standard ATA PCMCIA device and one Compact FLASH or MicroDrive site. Figure D1.4 illustrates the significant connectors for this device while Table D1.4 indicates the jumper settings for the various Master/Slave device configurations.

Figure D1.4 IPM-ATA-PCMCIA Board Layout

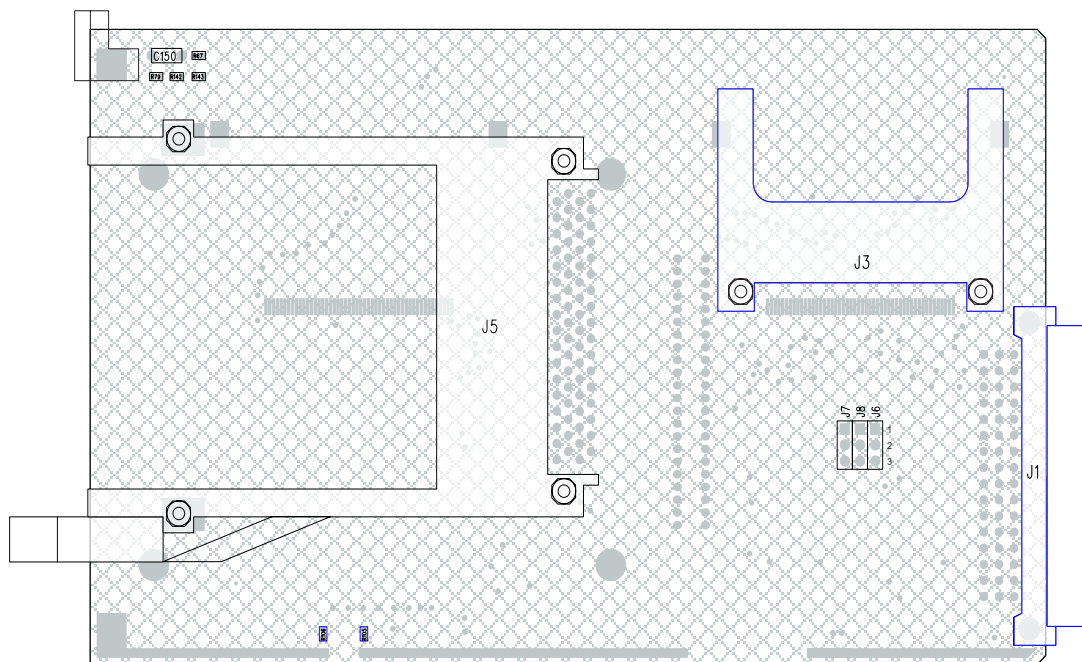


Table D1.4 IPM-ATA-PCMCIA Jumper Description

Jumper J8	PCMCIA Device in J5	Jumper J6	CompactFlash or MicroDrive in J3
2-3	Master	2-3	Master
Open	Slave	Open	Slave

It should be noted that the secondary IDE channel only (from rear I/O) is available for use by the IPM-ATA-PCMCIA (the primary is on the CPU board itself). Multi Master or multi Slave configurations are not supported and will not work!

**Note:**

*The PCMCIA device cannot and must not be removed during use. To exchange or remove the device, first power-down the system!*

## D1.5 Device Compatibility

Because of the diversity of Compact FLASH devices available with different architectures and error recovery routines etc. there is a strong possibility that some Master / Slave combinations will fail to be recognised by the BIOS. To help highlight the problem, Inova have provided the test report shown in Table D1.5 which should be regarded as a guide when choosing to pick-and-mix devices. Should devices other than those from the manufacturers indicated in the table be chosen, then it may be prudent that Inova be contacted prior to commissioning.

Table D1.5 Compatibility List

Test	Position	Compact FLASH Card	Jumper	Result
1	J3	IBM Microdrive DMDM-10340	Master	Passed
	J4	Empty	-	
2	J3	M-Systems 64MByte Compact FLASH	Master	Passed
	J4	Empty	-	
3	J3	IBM Microdrive DMDM-10340	Slave	Passed (incl. Strip Set Config.)
	J4	IBM Microdrive DMDM-10340	Master	
4	J3	IBM Microdrive DMDM-10340	Slave	Passed
	J4	M-Systems 64MByte Compact FLASH	Master	
5	J3	IBM Microdrive DMDM-10340	Master	Failed: M-Systems not detected in BIOS
	J4	M-Systems 64MByte Compact FLASH	Slave	
6	J3	M-Systems 64MByte Compact FLASH	Master	Passed
	J4	IBM Microdrive DMDM-10340	Slave	

### Note:

*This module only supports ATA PCMCIA cards (memory) and cannot be used with WLAN, modem, GPS etc. PCMCIA devices.*

*If one configuration seems not to work, try swapping Master and Slave.*

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# AGP-R7000

## AGP-R7000

### E1 AGP-R7000 CPU Extension..... E-2

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## E1 AGP-R7000 CPU Extension

The AGP-R7000 is an Inova AGP 4x ATI Radeon-based graphic extension for use with the ICP-P4, ICP-P4(M), ICP-PM and ICP-CM CPUs. By utilizing the power of the ATI Radeon 7000 equipped with 32MByte of SDRAM, a graphic performance improvement of some 50%<sup>1.)</sup> can be expected when compared to the on board (chipset) solution. Able to drive analog VGA or PanelLink compatible monitors directly or connect to the IBP-GS-MULTILINK GigaST★R transmitter with CAN routing for long-distance digital data transfer, the AGP-R7000 suits the demands of modern industrial (automation engineering) applications.

It is fabricated in 2 basic versions: Analog VGA or digital DVI-D (TMDS). Connectors J1, J3 and J5 are explained later in this section.

Table E1.00 AGP Piggyback Configurations

J1 (Front)	Rear I/O	J3 / J5	Option
CRT 1	-	TFT	Option 1
CRT 1	CRT 1	TFT	Option 2
CRT 1	CRT 2	TFT	Option 3
TMDS	-	TFT	Option 4
TMDS	CRT 1	TFT	Option 5

### Note

*The front and/or rear connected display devices may be configured to show the same or different (independent) video content to TFT units by configuring the driver software.*

*With the AGP installed, the onboard (chipset) graphic is disabled.*

*Options 2 and 5 are preferred (standard).*

*Option 3, although possible, should only be selected if CRT 1 is permanently connected.*

1.) OpenGL applications performed 83% faster with the AGP piggyback installed and memory efficiency increased by 14%

## E1.1 Specifications

<b>Interface</b>	AGP 4x (120-pin connector)		
<b>Video Controller</b>	ATI Radeon with 32MByte RAM		
<b>Screen Options (TFT &amp; VGA)</b>	Resolution	Colour Depth	Refresh
	1920 x 1200	32-bit	72Hz
	1920 x 1200	16-bit	80Hz
	2048 x 1536	16-bit	60Hz
<b>TMDS</b>	1600 x 1200	24-bit	60Hz
<b>Configuration</b>	DIP switch for DDC data or fixed resolution		
<b>User Interfaces</b>	15-pin D-Sub for front-panel VGA or 15-pin D-Sub for front-panel TMDS (PanelLink) 2x27 pin ZIF connector for TFT (GigaST★R)		
<b>Options</b>	Front or rear-panel VGA <sup>1)</sup> Front-panel TMDS and rear-panel VGA <sup>2)</sup>		
<b>Software Support</b>	Windows® 2000®, Windows® XP®		
<b>Power Req.</b>	+3.3V (2W), +5V (2W) (typically)		
<b>Mass</b>	40g (typically)		
<b>Oper. Temp.</b>	0°C to +60°C		
<b>Storage Temp.</b>	-40°C to +85°C		
<b>Humidity</b>	5% to 95% (non-condensing) @ 40°C		
<b>Warranty</b>	Three-year limited warranty		

<sup>1)</sup> Two VGA monitors can be connected simultaneously with identical video information on both - the Radeon graphics engine must be configured accordingly. An alternative is also available where the content appearing on the 2nd display is different to that of the first. The disadvantage of this configuration is that if a monitor is not connected to the front-panel (CRT1) the video content cannot be displayed on CRT2 (rear) until the OS has been initialised and the video driver initialised. If a BIOS upgrade is required or the settings need to be altered etc. then, without the CRT on the front-panel, the user will not see anything which makes the task almost impossible!

<sup>2)</sup> This is the only supported mode whereby (independent) video can be produced via the front DVI-D and a rear connected analog (CRT) device.

Both options support TFT - video content can be selected to be the TMDS or CRT

## E1.2 J4 Interface

Communication to and from the host CPU is through J4 (refer to figure E1.20) - the AGP interface. The video output, as discussed earlier, is hardware configured (at time of purchase) for different front and rear panel modes - refer to table E1.00. The TFT option (J3/J5) is always present.

The J4 AGP interface on the graphic piggyback is electrically identical to AGP, but has a smaller form factor and uses a different connector. Table E1.20 shows the pinout of this connector.

*Figure E1.20 J4 on the Underside of the AGP-R7000 Piggyback*

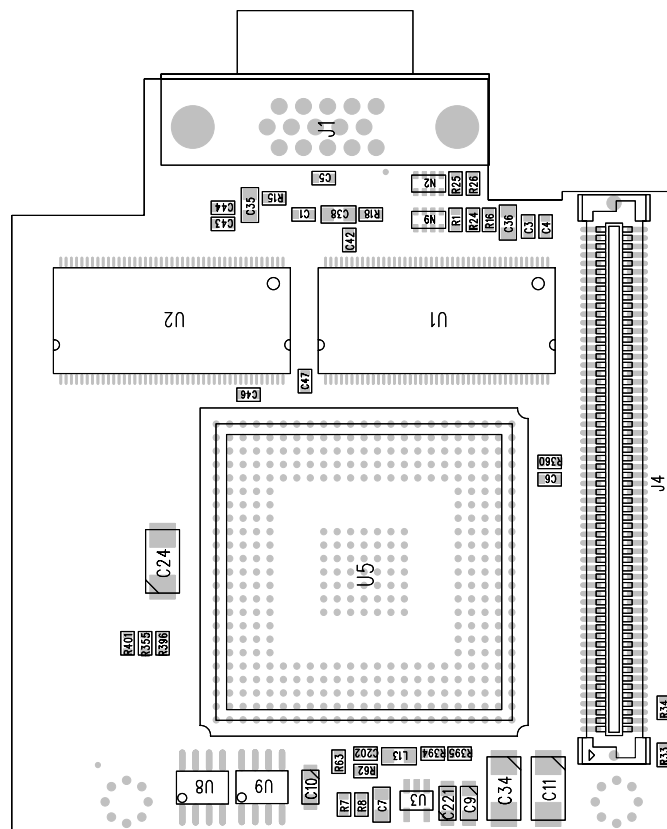




Table E1.20 J4 Pinout

Pin No.	Signal	Pin No.	Signal
1	USB6+	2	GND
3	PC_BEEP	4	USB6-
5	VCC3.3	6	AC_RESET#
7	SYNC	8	BITCLK
9	SDATA_OUT	10	VCC5
11	INTB#	12	SDATA_IN
13	GND	14	INTA#
15	CLK	16	RST#
17	REQ#	18	GND
19	ST0	20	GNT#
21	VCC3.3	22	ST1
23	ST2	24	-
25	RBF#	26	VCC3.3
27	-	28	PIPE#
29	GND	30	WBF#
31	SBA0	32	SBA1
33	SBA2	34	GND
35	SB_STB	36	SBA3
37	VCC3.3	38	SB_STB#
39	SBA4	40	SBA5
41	SBA6	42	VCC3.3
43	AD31	44	SBA7
45	GND	46	AD30
47	AD29	48	AD28
49	AD27	50	GND
51	AD25	52	AD26
53	VDDQ1.5	54	AD24
55	AD_STB1	56	AD_STB1#
57	AD23	58	VDDQ1.5
59	AD21	60	C/BE3#

Table E1.20 J4 Pinout - Contd.

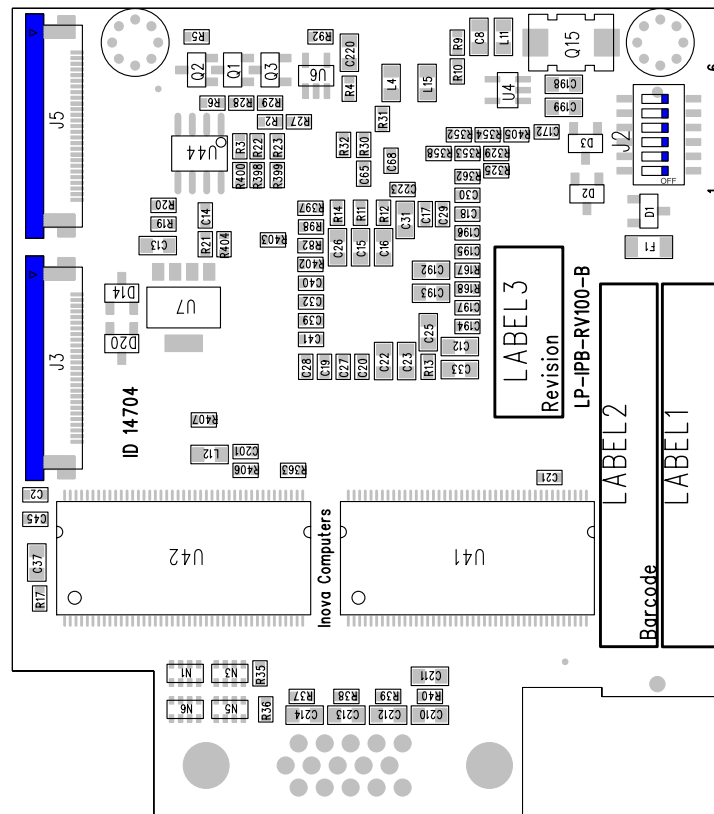
Pin No.	Signal	Pin No.	Signal
61	GND	62	AD22
63	AD19	64	AD20
65	AD17	66	GND
67	C/BE2#	68	AD18
69	VDDQ1.5	70	AD16
71	IRDY#	72	FRAME#
73	DEVSEL#	74	VDDQ1.5
75	-	76	TRDY#
77	GND	78	STOP#
79	PERR#	80	PME#
81	SERR#	82	GND
83	C/BE1#	84	PAR
85	VDDQ1.5	86	AD15
87	AD14	88	AD13
89	AD12	90	VDDQ1.5
91	AD10	92	AD11
93	GND	94	AD9
95	AD8	96	C/BE0#
97	AD_STB0	98	GND
99	AD7	100	AD_STB0#
101	VDDQ1.5	102	AD6
103	AD5	104	AD4
105	AD3	106	VDDQ1.5
107	AD1	108	AD2
109	GND	110	AD0
111	VREFCG	112	VREFGC
113	VGA_R	114	GND
115	VGA_G	116	HSYNC
117	GND	118	VSYNC
119	VGA_B	120	VB_EN

## E1.3 J3 & J5 IBP-GS-MULTILINK (TFT) Interfaces

To address an almost unlimited number of cascaded digitally connected (GigaST★R) TFT displays with optional CAN control and Panellink Slave connectivity, the Inova GigaST★R transmitter piggyback, IPB-GS-MULTILINK needs to be installed adjacent to the AGP piggyback. This connection is made through connectors J3 and J5 on the upper side of the piggyback as shown in figure E1.30. Table E1.30 gives the pinout of these two connectors.

The settings of the DIP switch (J2) are explained later.

Figure E1.30 J3 and J5 Topside Connectors for the Inova IPB-GS-MULTILINK



Also visible on the upper side of this piggyback are three labels - one (Label 1) shows the name of the board, the second shows the product bar code (with manufacturing details, lot number and ID number) and the third (Label 3) carries the revision number. The board revision is also printed on the PCB.

*Table E1.30 J3 & J5 Interface Pinout*

J3 Connector		J5 Connector	
Pin No.	Signal	Pin No.	Signal
1	D16_R0	1	D0_B0
2	D17_R1	2	D1_B1
3	GND	3	GND
4	D18_R2	4	D2_B2
5	D19_R3	5	D3_B3
6	GND	6	GND
7	D20_R4	7	D4_B4
8	D21_R5	8	D5_B5
9	GND	9	GND
10	D22_R6	10	D6_B6
11	D23_R7	11	D7_B7
12	GND	12	GND
13	CLK	13	D8_G0
14	GND	14	D9_G1
15	DE	15	GND
16	GND	16	D10_G2
17	HSYNC	17	D11_G3
18	GND	18	GND
19	VSYNC	19	D12_G4
20	GND	20	D13_G5
21	GND	21	GND
22	GND	22	D14_G6
23	VCC3.3	23	D15_G7
24	VCC3.3	24	VCC5.0
25	VCC3.3	25	VCC5.0
26	VCC3.3	26	VCC5.0
27	VCC3.3	27	VCC5.0

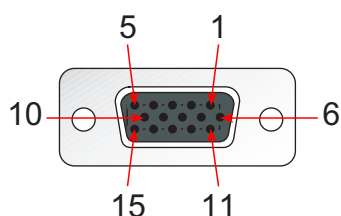
Information on the GigaSTAR IPB-GS-MULTILINK can be found in the respective documentation.

### E1.4 J1 Front-Panel VGA/TMDS Interface

Standard analog VGA or digital (PanelLink) monitors can be connected to the AGP-R7000 via the 15-pin, D-Sub J1 interface. A bank of DIP switches (J2) enables the resolution of connected TFT or TMDS displays to be set or permits the system software to access the DDC data from standard analog or digital TMDS devices and set the resolution automatically.

Figure E1.40 shows the VGA/TMDS connector signals for the front-panel D-Sub connector and tables E1.40 to E1.42 show the connector pinout and DIP switch settings respectively.

Figure E1.40 Standard Front-Panel VGA/TMDS Interface



**Note:**

A 3m length of 9-pin D-Sub to DVI-D cable is supplied with each CPU configured with this graphic option.

Table E1.40 J1 Standard Front-Panel VGA/TMDS Pinout

Pin No.	Analog (CRT) Signal	Digital (TMDS) Signal
1	Analog RED	TX2#
2	Analog GREEN	TX1#
3	Analog BLUE	TX0#
4	N/C	TXC#
5	N/C (GND)	DDC_DAT
6, 8	GND	GND
7	N/C (GND)	USB_D+
9	+5V	+5V
10	N/C (GND)	USB_D-
11	N/C	TX2
12	DDC_DAT	TX1
13	HSYNC	TX0
14	VSYNC	TXC
15	DDC_CLK	DDC_CLK

*Table E1.41 J2 DIP Switch Settings - Digital TMDS (Panellink) or DVI-D*

SW3	SW2	SW1	Resolution	Comments
OFF	OFF	OFF	Disabled	See Note Below
OFF	OFF	ON	640 x 480	60Hz
OFF	ON	OFF	800 x 600	60Hz
OFF	ON	ON	1024 x 768	60Hz
ON	OFF	OFF	1280 x 1024	60Hz
ON	OFF	ON	Reserved	
ON	ON	OFF	Reserved	
ON	ON	ON	Reserved	

*Table E1.42 J2 DIP Switch Settings - TFT (24Bit TTL/CMOS)*

SW6	SW5	SW4	Resolution	Comments
OFF	OFF	OFF	Disabled	
OFF	OFF	ON	Reserved	
OFF	ON	OFF	800 x 600	
OFF	ON	ON	1024 x 768	60Hz
ON	OFF	OFF	Reserved	
ON	OFF	ON	Reserved	
ON	ON	OFF	Reserved	
ON	ON	ON	Reserved	

**Note:**

*If an external DDC is found then the switch settings SW1 to SW3 have no effect. This applies to the digital TMDS configuration only*

**Note:**

*If the AGP piggyback is installed, the VGA connector associated with the chipset graphic must be removed. For this reason, the AGP piggyback is NOT available as an accessory to be added as an after thought!*

## **E1.5 Rear I/O VGA Interface**

Refer to the rear I/O documentation for video interfacing connectivity.